CSI RD&D Project Webinar

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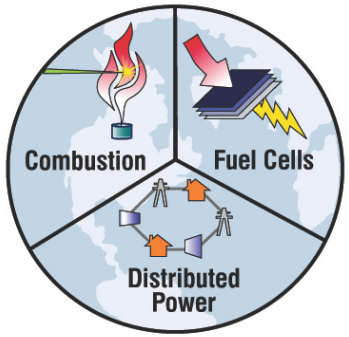


In Collaboration with PG&E

June 4, 2013

Project Goals

Develop modeling tools to simulate distribution circuits

Collaborate with Pacific Gas & Electric to acquire, analyze, and evaluate circuit performance data from circuits with high-pen PV

Systematically utilize the modeling tools in combination with the field data to

- Quantify PV integration limitations
- Develop and evaluate progressively smarter systems for handling high-pen PV

Tasks & Key Deliverables

Task 1 Project management

Task 2 Model development and evaluation

- Model scenarios and comparisons to grid monitored data

Task 3 Quantify PV integration limits

- Determine limits for PV penetration within existing circuit architectures and with existing technology

Task 4 Advanced inverter control

- Assess the risks and benefits of advanced inverter control

Task 5 Integrated distribution grid control

- Progressively introduce and assess smart integrated distribution technologies/ controls to determine impacts on PV penetration

Task 6 Practical feasibility and outreach

- Determine market potential of technology and encourage adoption

Task 2 Model Development and Evaluation

Commercial Circuit (Cayetano)

21 kV Wye

Demand

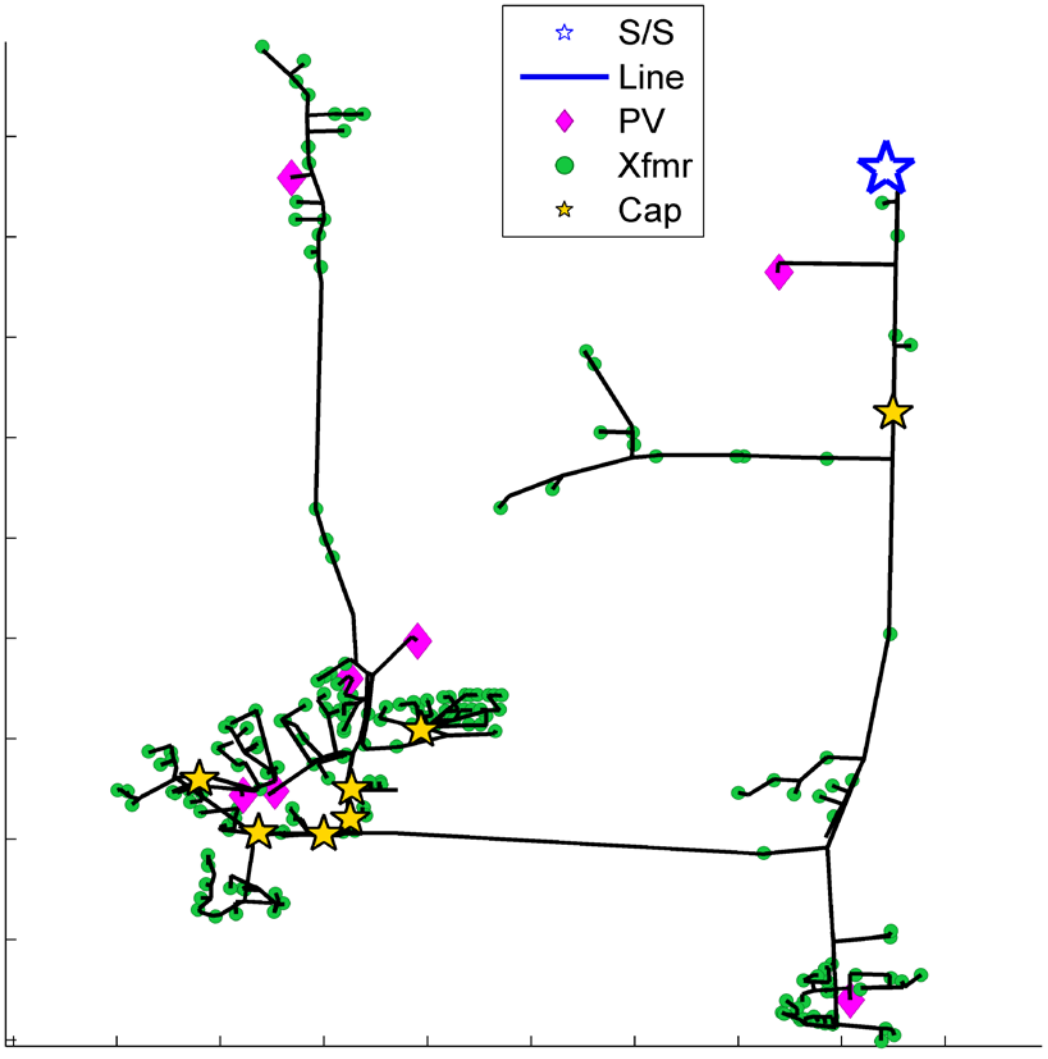
- 12 MW max
- 1202 customers (237 Xfmrs)
- 91.2% energy for Commercial & Industrial customers

PV Generation

- 1.873 MW (15.6% penetration)
- 7 installations (2 > 500kW)

Equipment

- LTC (45 MVA, 10% regulation)
- 7 switched capacitors (9.6 MVAR)



Task 2 Model Development and Evaluation

Residential Circuit (Menlo)

12 kV Delta

- Two 4.16kV Wye sections

Demand

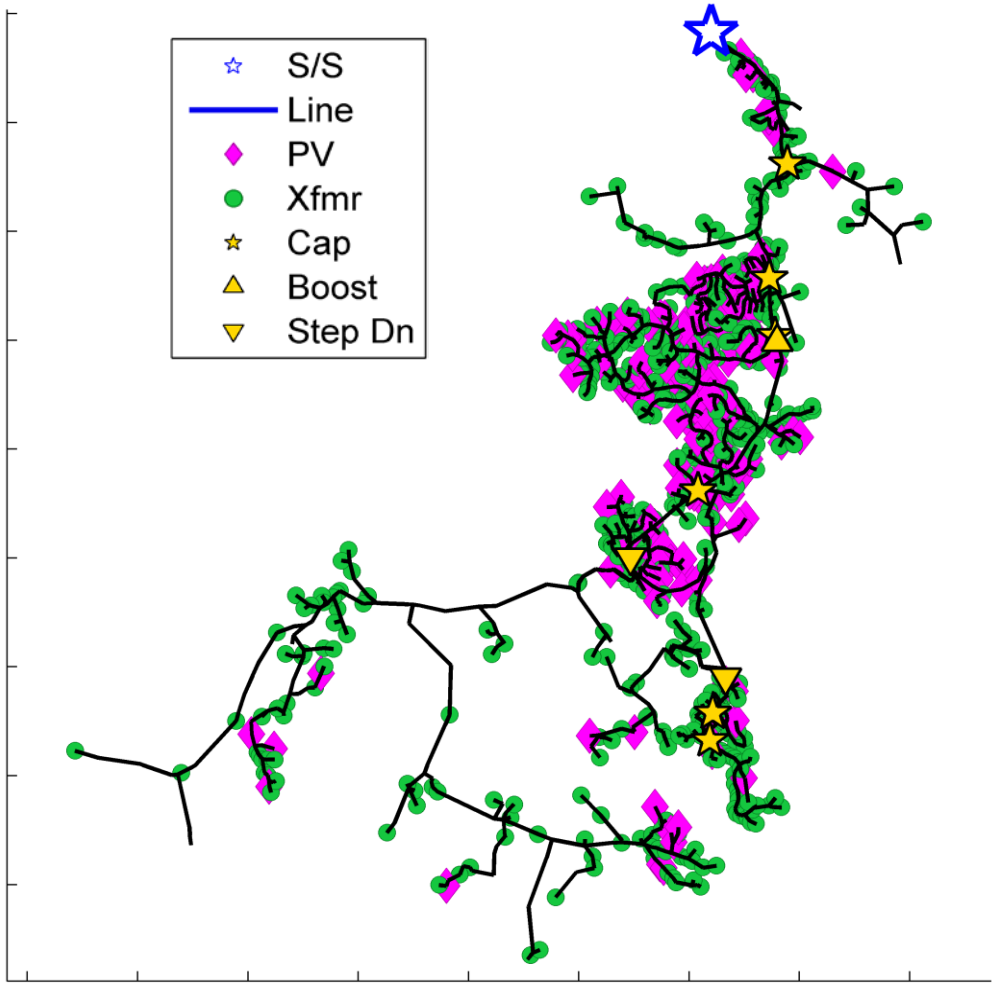
- 9.1 MW max
- 2681 customers (827 Xfmrs)
- 73.7% Domestic customers

PV Generation

- 1.105 MW (12.1% pen)
- 165 installations (163 < 50kW)

Equipment

- LTC (16MVA, 10% regulation)
- 4 sw'd, 2 fx'd Capacitors (3.6 MVAR)
- Booster (5.16 MVA, +3%)
- 2 Step-Downs (1 and 0.75 MVA)

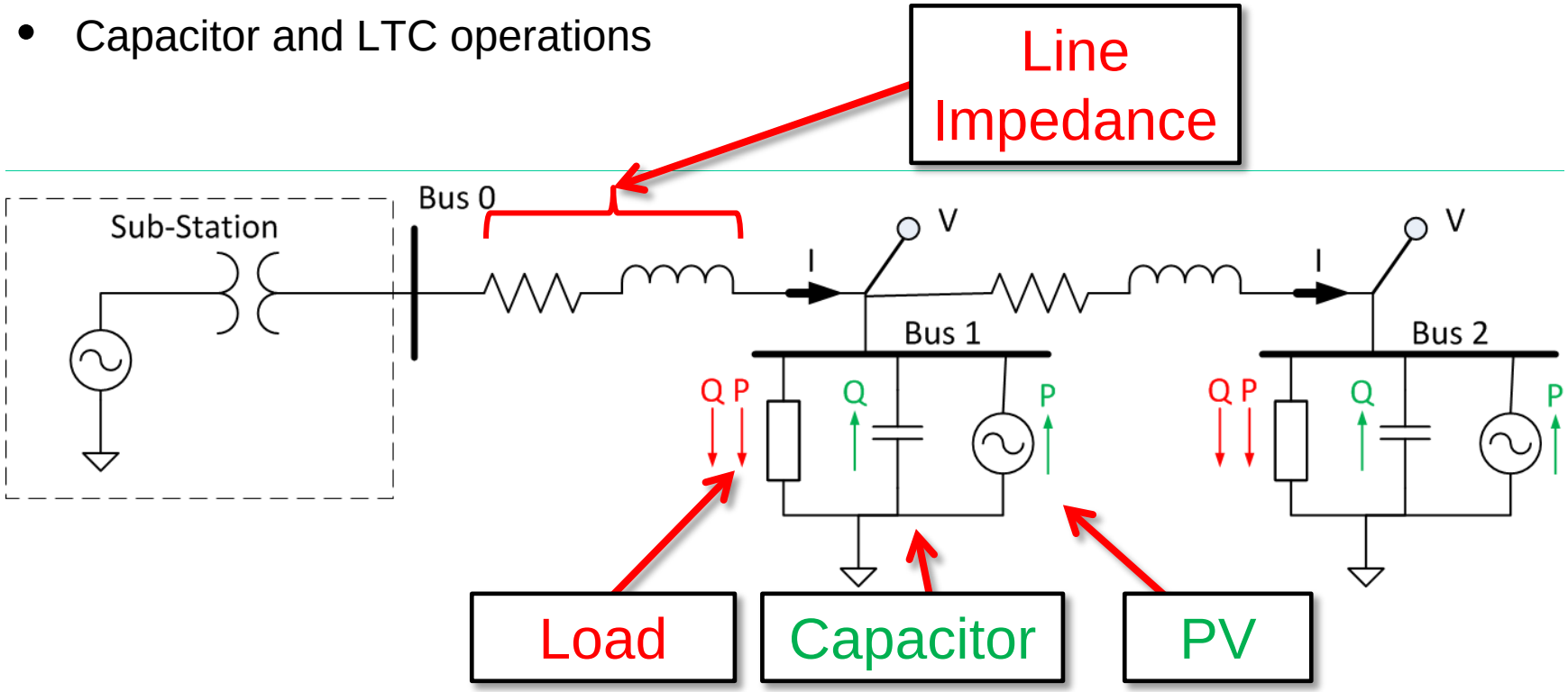


Task 2 Model Development and Evaluation

Balanced 3-Phase Feeder Model

Steady-State voltage behavior on the primary feeder

- Time Resolved Load (distributed SCADA) and Generation (SolarAnywhere est.)
- Voltage Drop between buses
- Capacitor and LTC operations

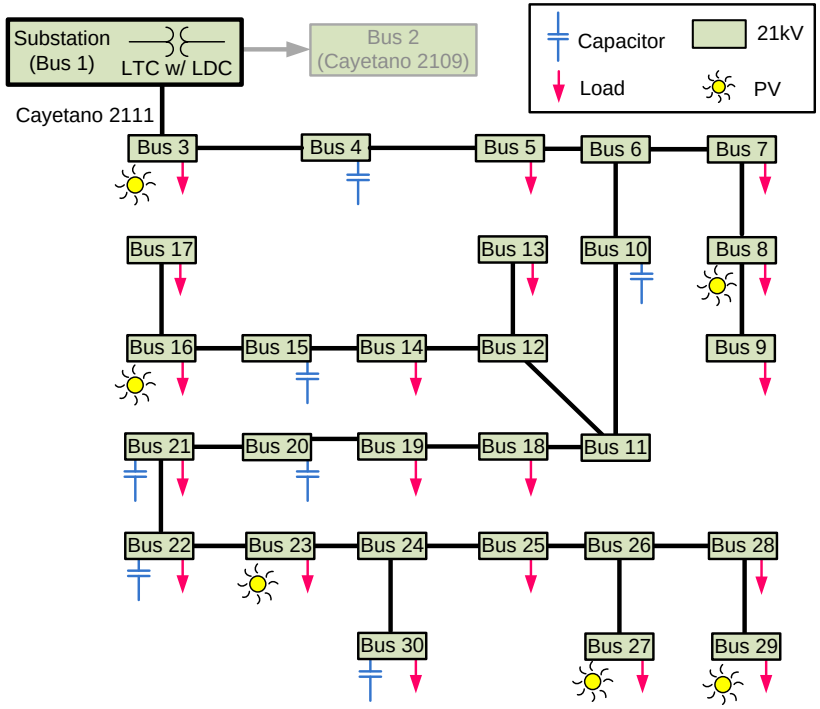


Does NOT provide information about Power Quality and Protective Devices

Task 2 Model Development and Evaluation

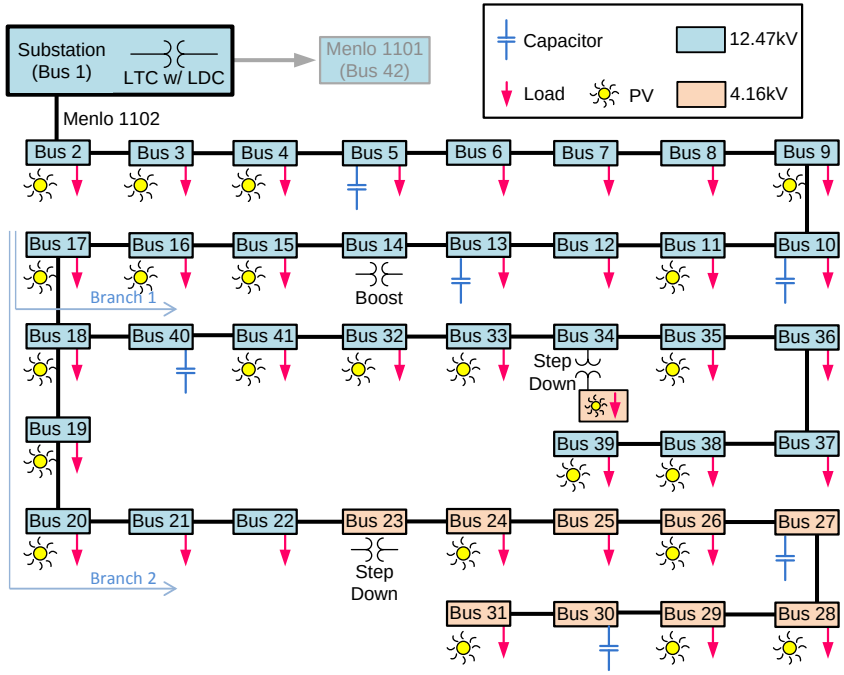
Commercial Circuit (Cayetano)

- 29 bus balanced feeder model
- OLTC with LDC
- 7 switching capacitors
  - Time-Clock, Temperature, Voltage Override
- 7 buses with PV generation



Residential Circuit (Menlo)

- 40 bus balanced feeder model
- OLTC with LDC
- 6 switching capacitors
  - Time-Clock, Temperature, Voltage Override
- 23 buses with PV generation
- 3% Boost Transformer
- 2 Step-down Transformer



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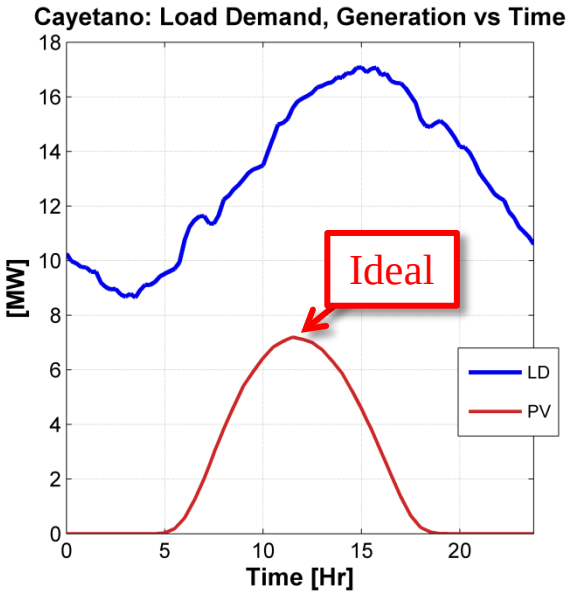
Task 3 Quantify PV Integration Limits

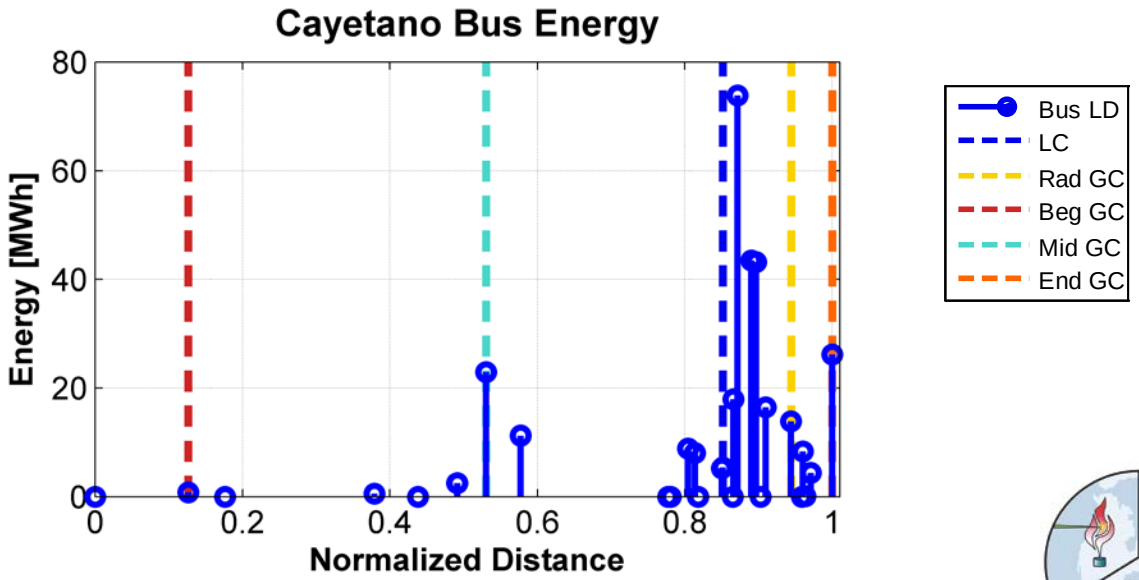
Determine limits for PV penetration within existing circuit architectures and with existing technology

- ① Voltage Control Equipment, ② Voltage, ③ Power Factor, ④ Line Loss

Scenarios

- **Penetration**: 0 – 100% Nameplate Penetration
- **Spatial Distributions**: Radial (new PV placed on existing buses with PV), Beginning, Middle, End
- **Characteristic Demand Day**: Seasonal High and Low





Task 3 Concepts: Load/Generation Distribution

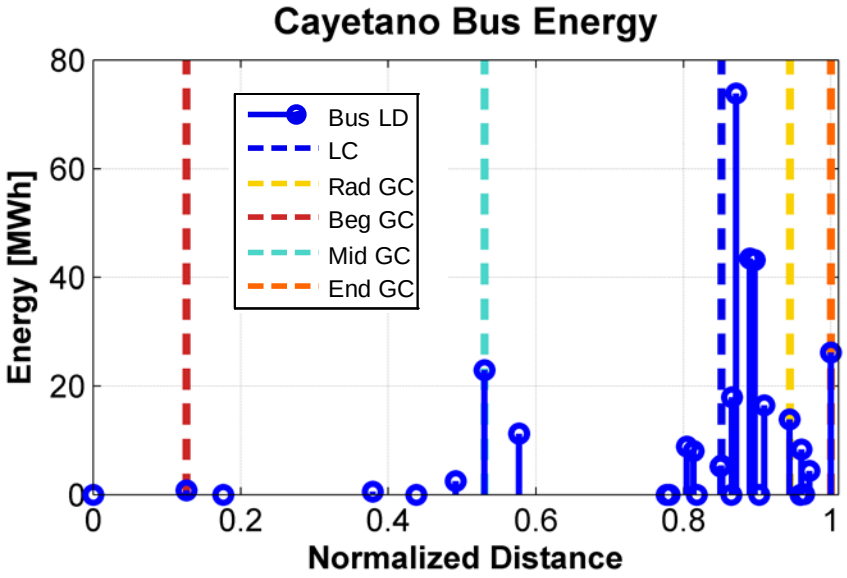
The Load Center (LC) is the average of bus load demand energy weighted by the normalized distance from the Sub-Station.

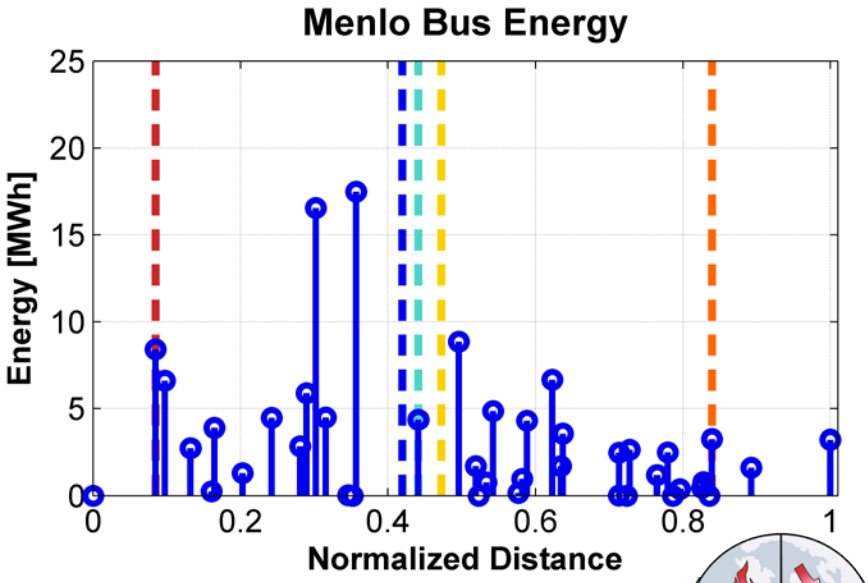
$$Load\ Center = \frac{\sum_i E_{LD,i} d_i}{\sum_i E_{LD,i}}$$

The Generation Center (GC) is the average of bus PV generation energy weighted by the normalized distance from the Sub-Station.

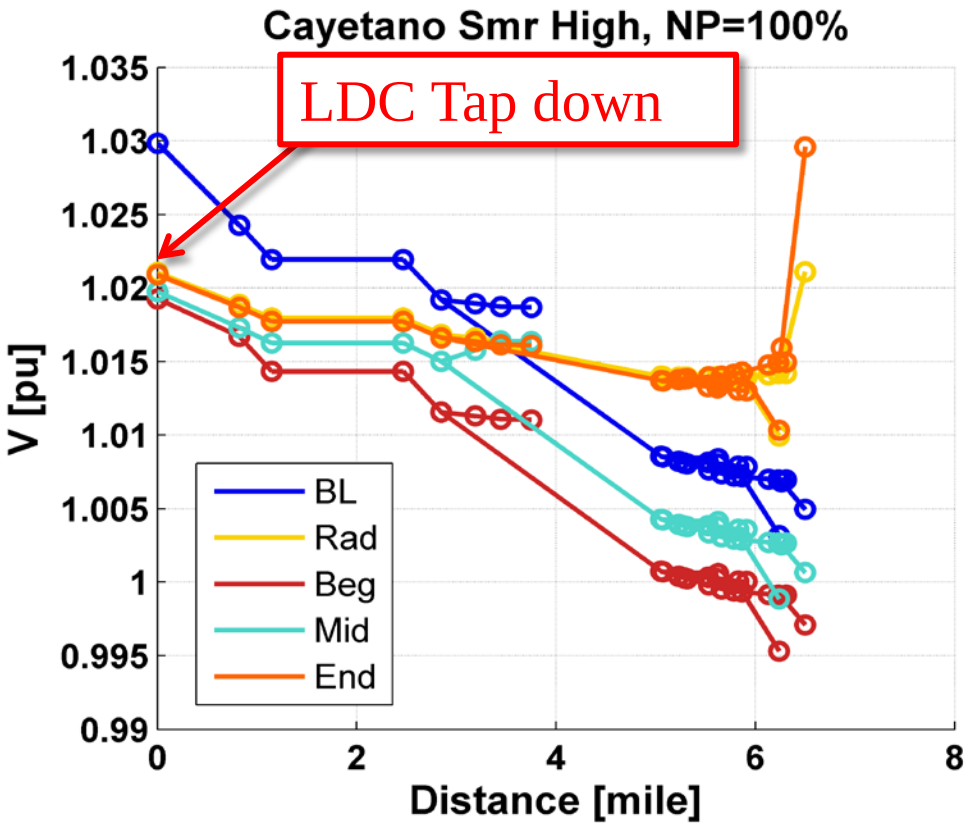
$$Generation\ Center = \frac{\sum_i E_{PV,i} d_i}{\sum_i E_{PV,i}}$$

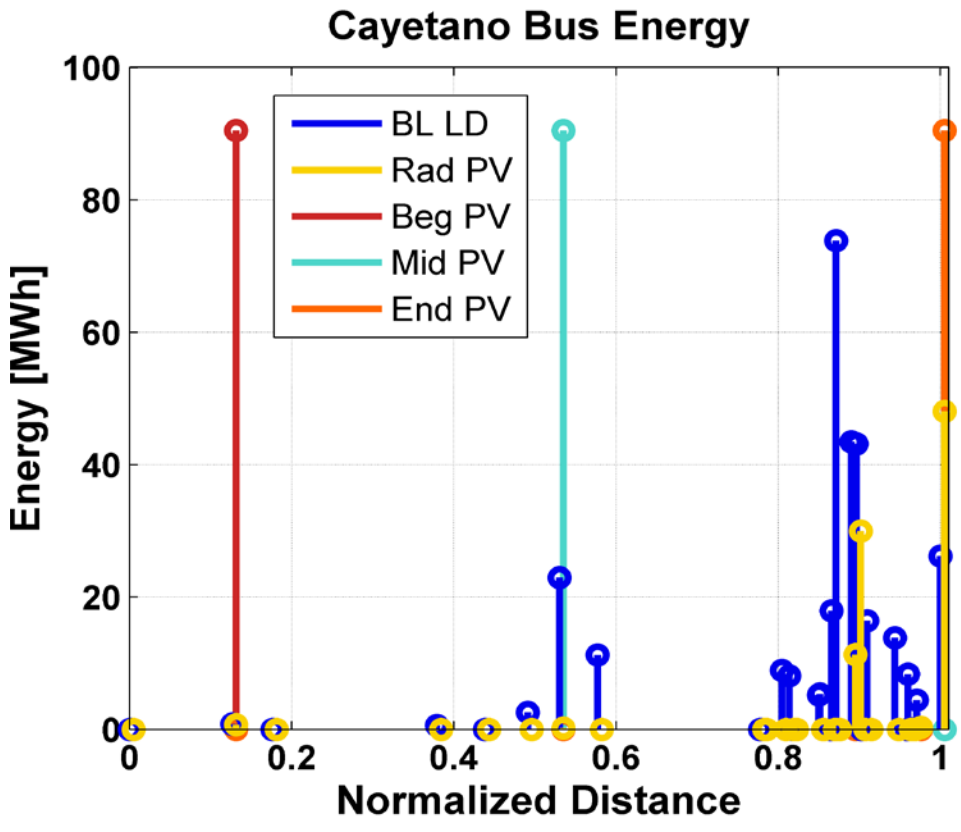
- $i = 1,2,\ldots,Total\ Bus\ Count$
- $E_{LD,I} = Total\ Day\ Energy\ consumed\ at\ Bus\ "i"$
- $E_{PV,I} = Total\ Day\ Energy\ generated\ at\ Bus\ "i"$





Task 3 Voltage Control Equipment: LDC



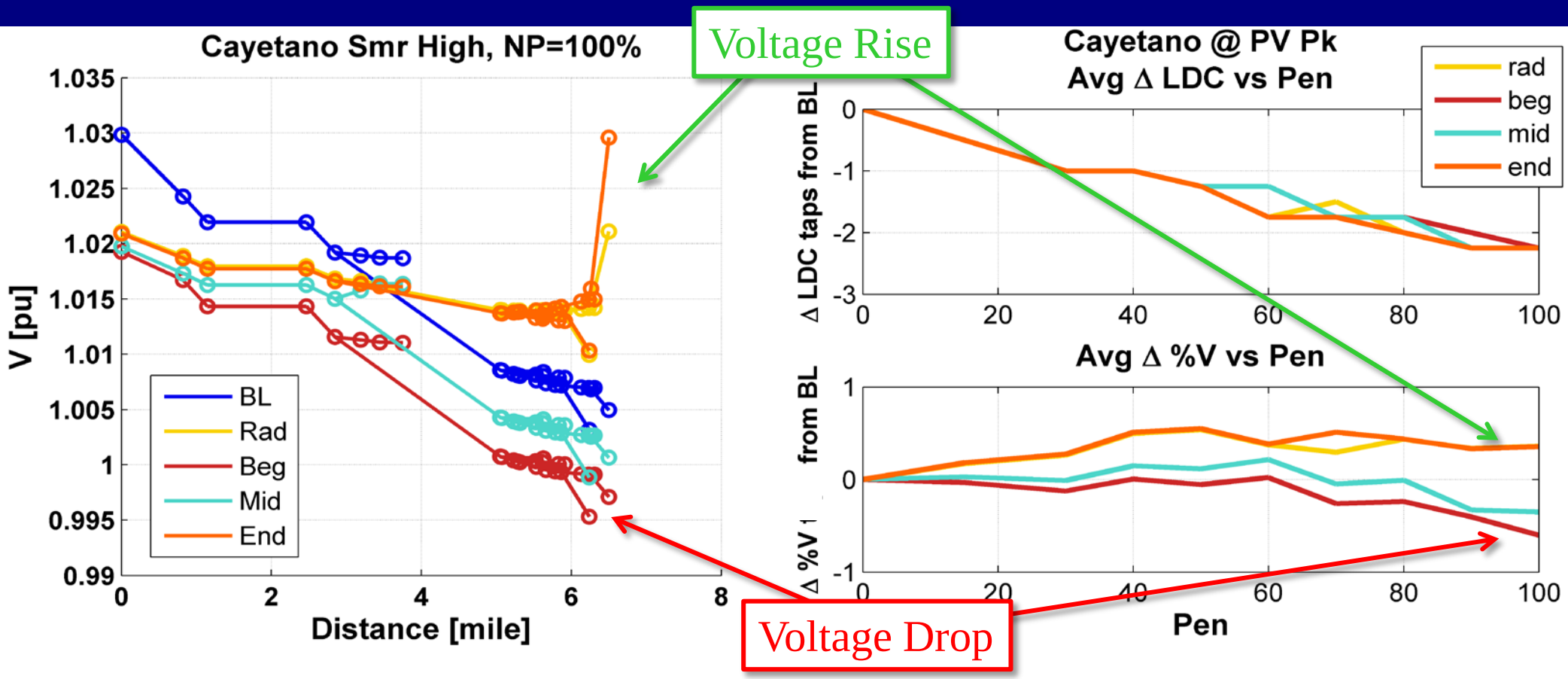


PV Generation support decreases net demand observed at Sub-Station

- LDC taps down

Spatial distribution affects LDC operation. In some instances, voltages outside of standards may occur if no mitigating actions are taken.

Task 3 Voltage Control Equipment: LDC



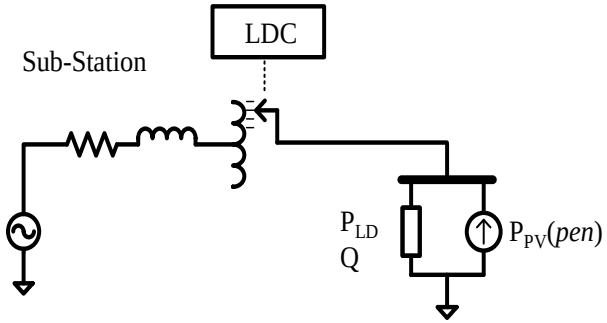
As PV Penetration increases

- Ending PV Distributions trend to voltage rise → in these cases LDC decreases voltage rise
- Beginning PV Distributions trend to voltage drop → in these cases LDC increases voltage drop

NOTE: Cayetano Summer High day did not have out of standard voltages, but demonstrates the trends caused by the interaction of the LDC and High Pen PV.

Task 3 Voltage Control Equipment: LDC

LDC "Tapping-Down" behavior consistent between all generation distributions.

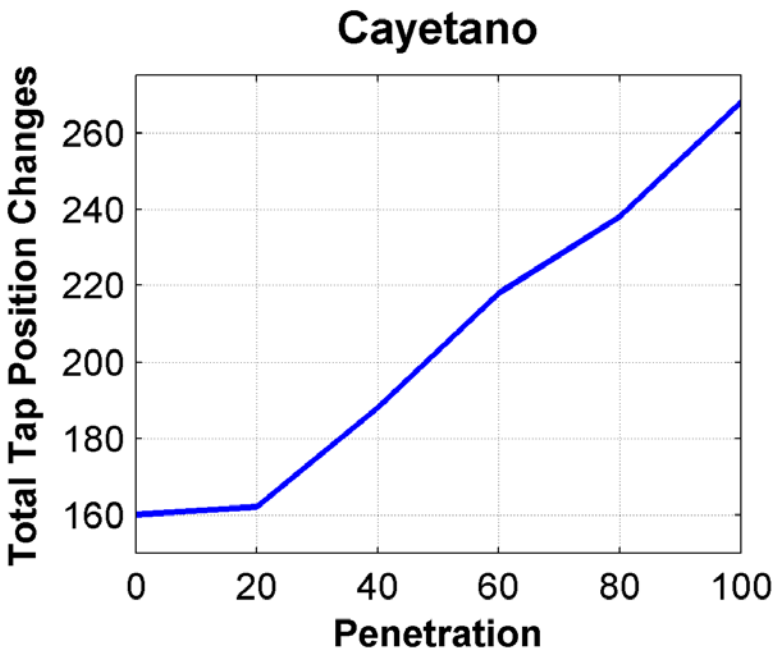


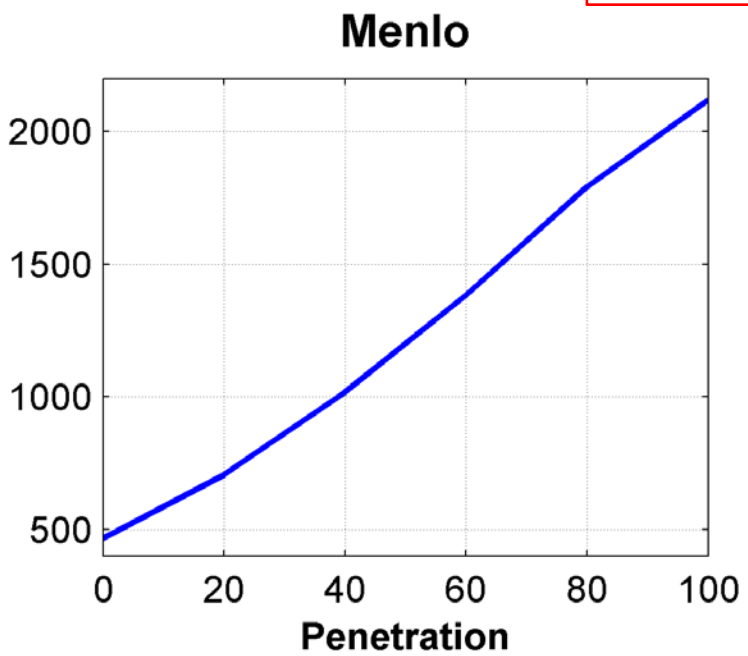
Modeling circuit load demand as a point source, we can simulate LDC total tap changes the versus PV penetration.

As PV penetration increases, total tap operations increases

- 20% to 100%: Cayetano 1.3 taps/pen
  Menlo 16.5 taps/pen

NOTE: Difference in tap/pen rate due to Current Transformer ratio and system voltage





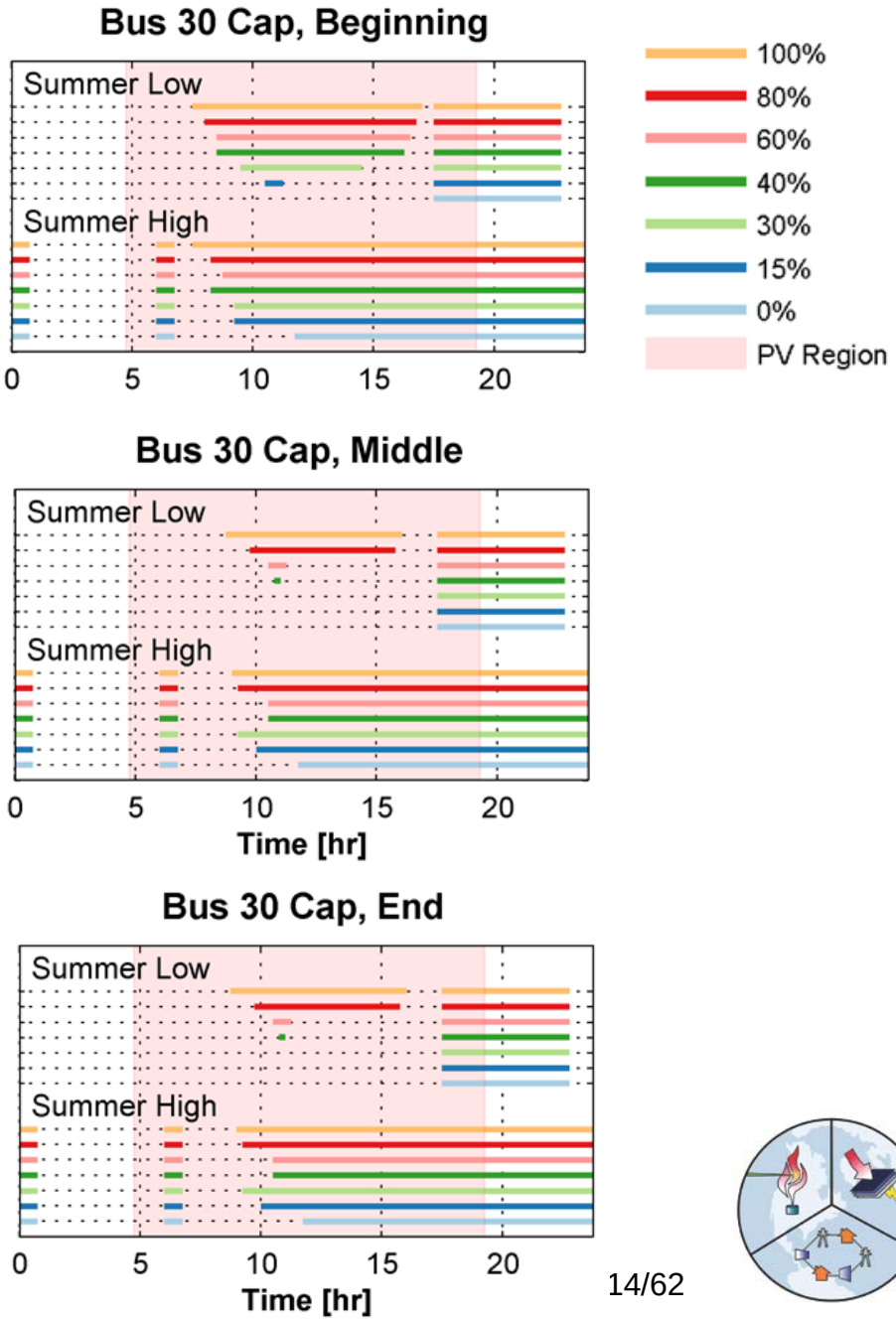
Task 3 Voltage Control Equipment: Capacitors

Cayetano and Menlo circuits featured Time-Clock and Voltage Override capacitor switching controls

Baseline (0%) switching behavior did not change in majority of scenarios.

- Menlo Summer Low days Bus 30 the **exception** (TC with VO)
- Bus 30 is located at end of Menlo circuit. LDC decreasing system voltage results in Low Voltage condition (Capacitor switches on)

High Pen PV has minimal impact on capacitor switching for circuits with LTC with LDC.



Task 3 Voltage

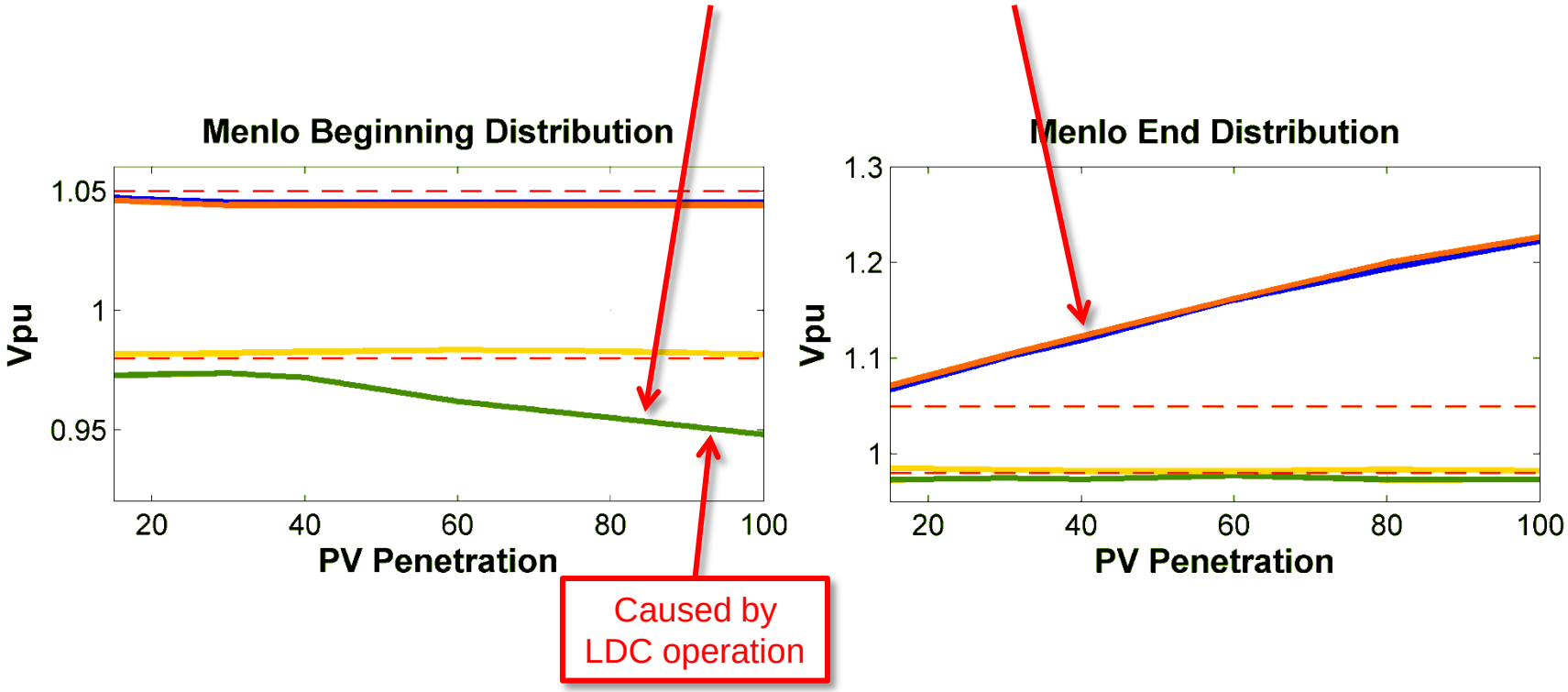
Bus Voltage evaluated to ANSI C84.1 (Range A)

- 1.05 – 0.95 V_{pu} → *Factor of Safety* → **1.05 – 0.98 V_{pu}**

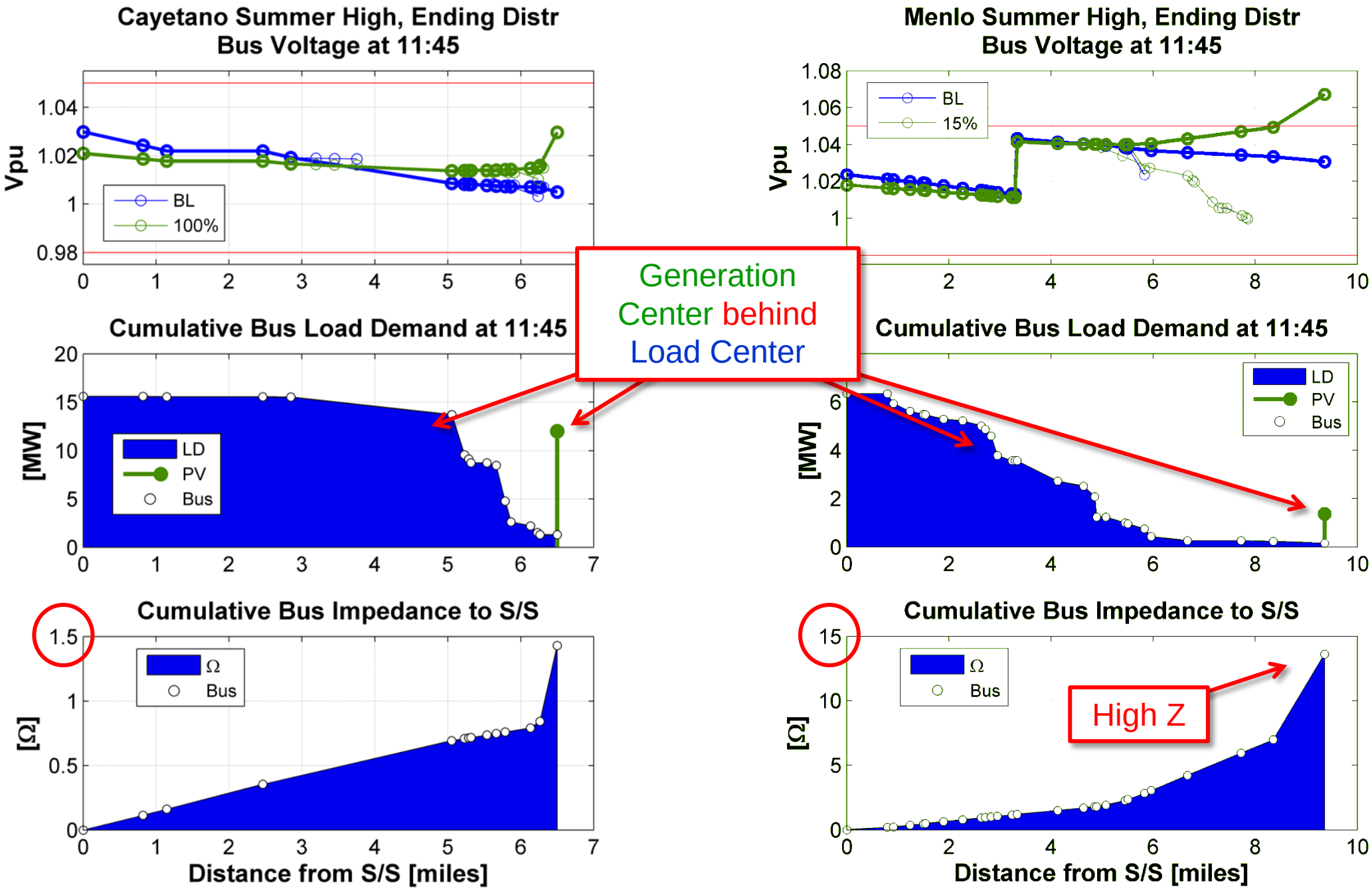
Cayetano: No bus voltage problems for all cases

- Primarily employs heavy conductor (low impedance)

Menlo: Voltage problems for beginning and ending distribution cases



Task 3 Voltage: High Voltage



Task 3 Voltage: High Voltage

Likelihood of exceeding voltage standard increases when:

- Excess generation at lower penetrations
- High impedance between GC and LC
- Aggravated by high line impedance to the adjacent upstream bus.

- Siting PV to avoid exceeding voltage standard is important (see siting criteria below).

Circuit	Distribution	LC/GC	Summer High RPF Pen	Initial Ω Upstream	Vmax [pu]
Menlo	End	0.42	1.7%	13.51	**1.24**
	Mid	0.95	25.7%	1.5	**1.04**
Cayetano	End	0.85	10.9%	1.46	**1.03**

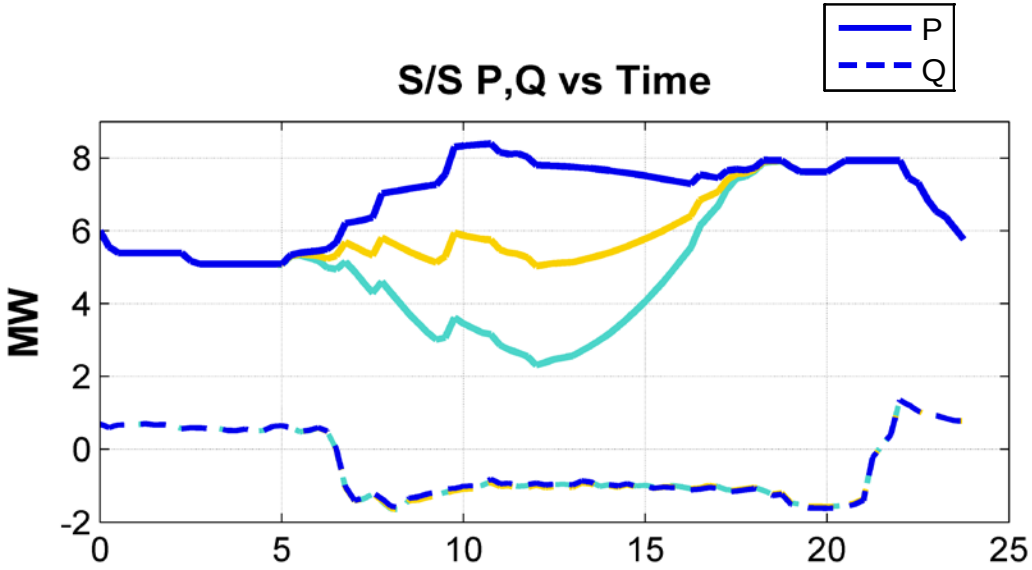
Task 3 Power Factor

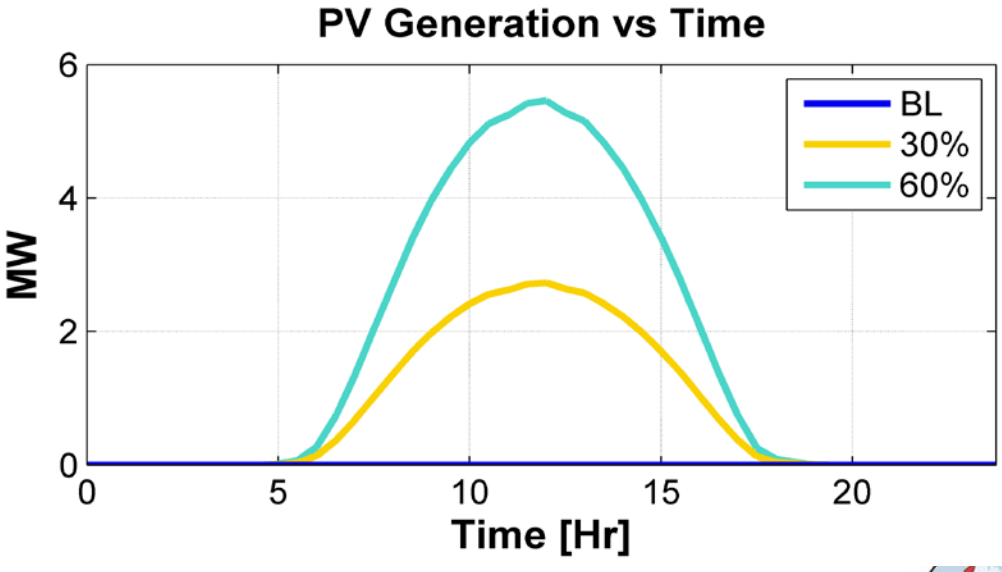
PV Generation provides real power support

As PV Penetration increases, the power factor at Sub-Station will decrease

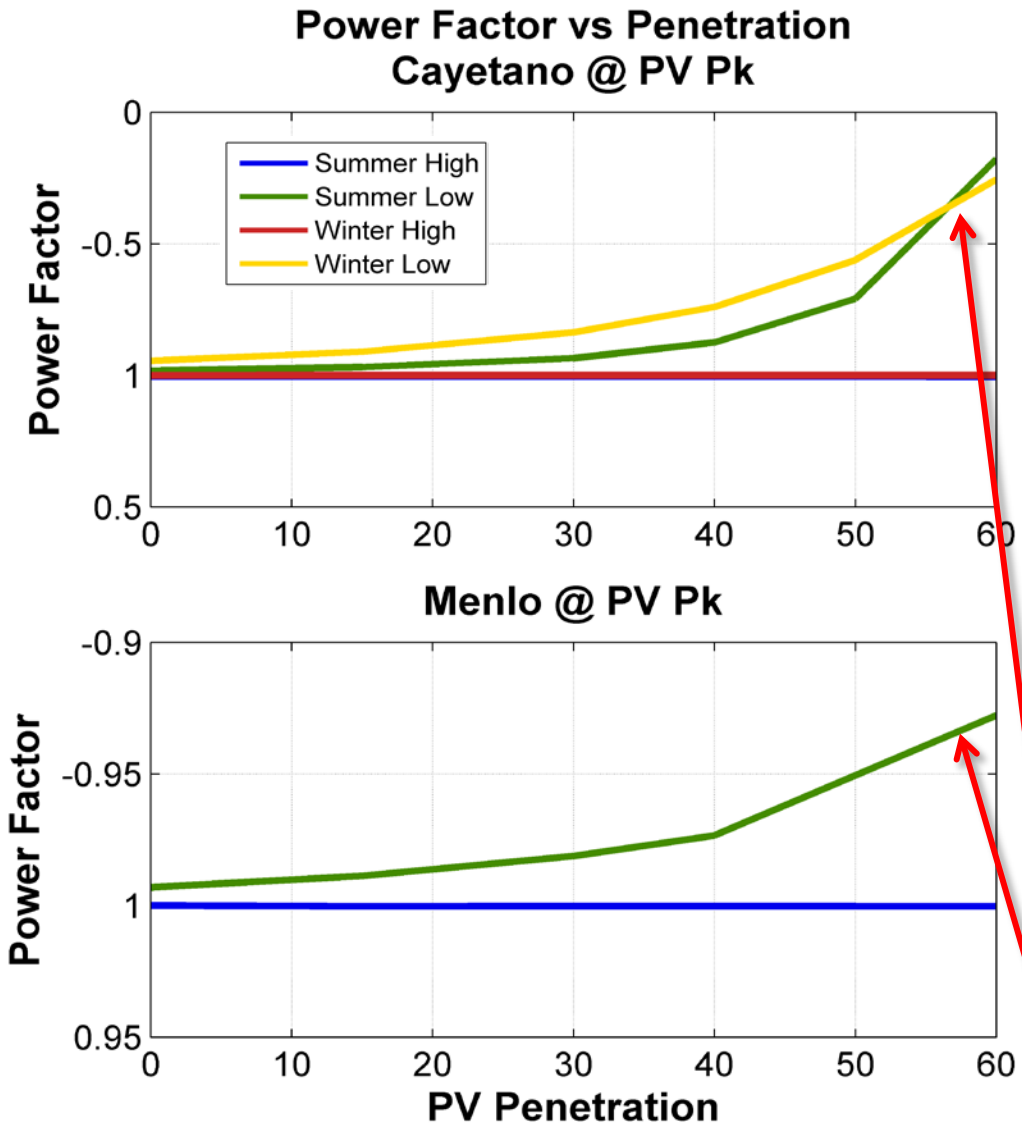
Impact

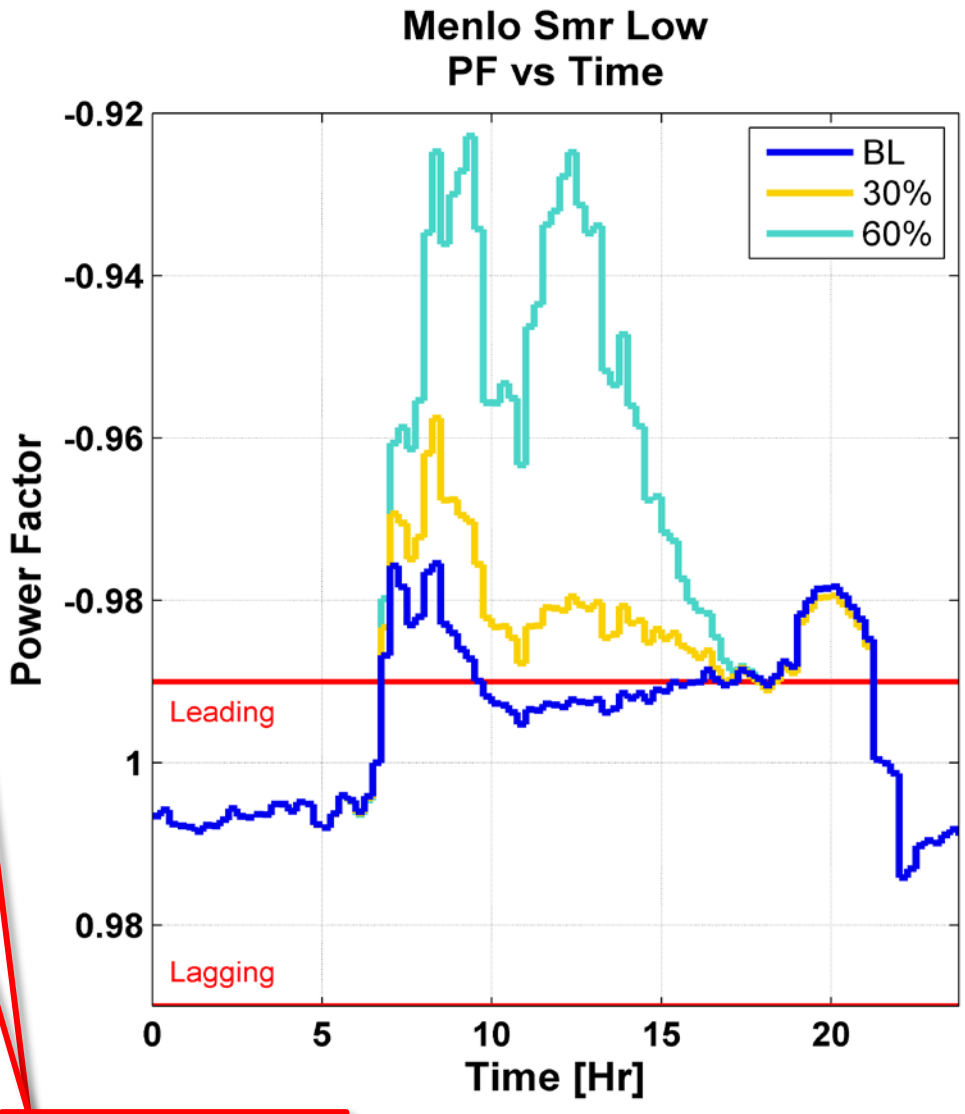
- High demand → marginal
- Low demand → sensitive





Task 3 Power Factor





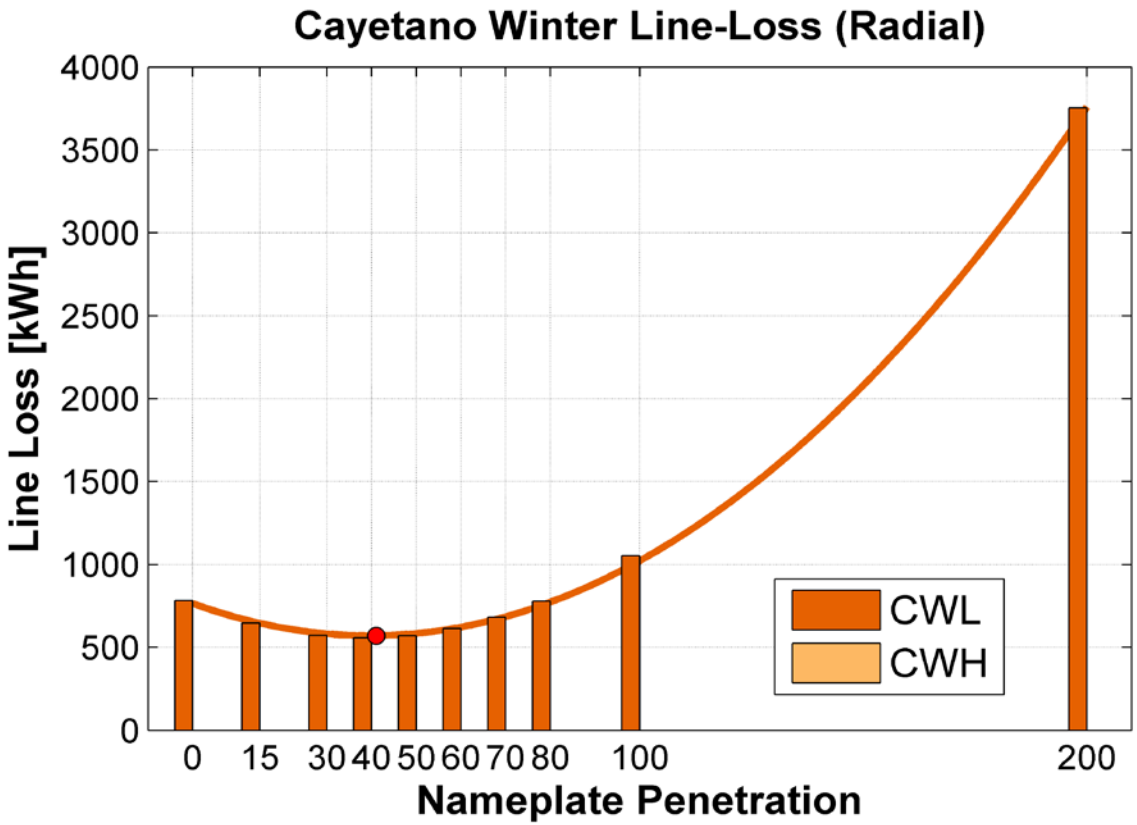
Decrease in PF for Low Days

Task 3 Line Loss

PV Generation is providing local demand support

- As Penetrations increase, S/S current draw decreases

I^2R Line loss has quadratic dependence on penetration



Task 3 Line Loss

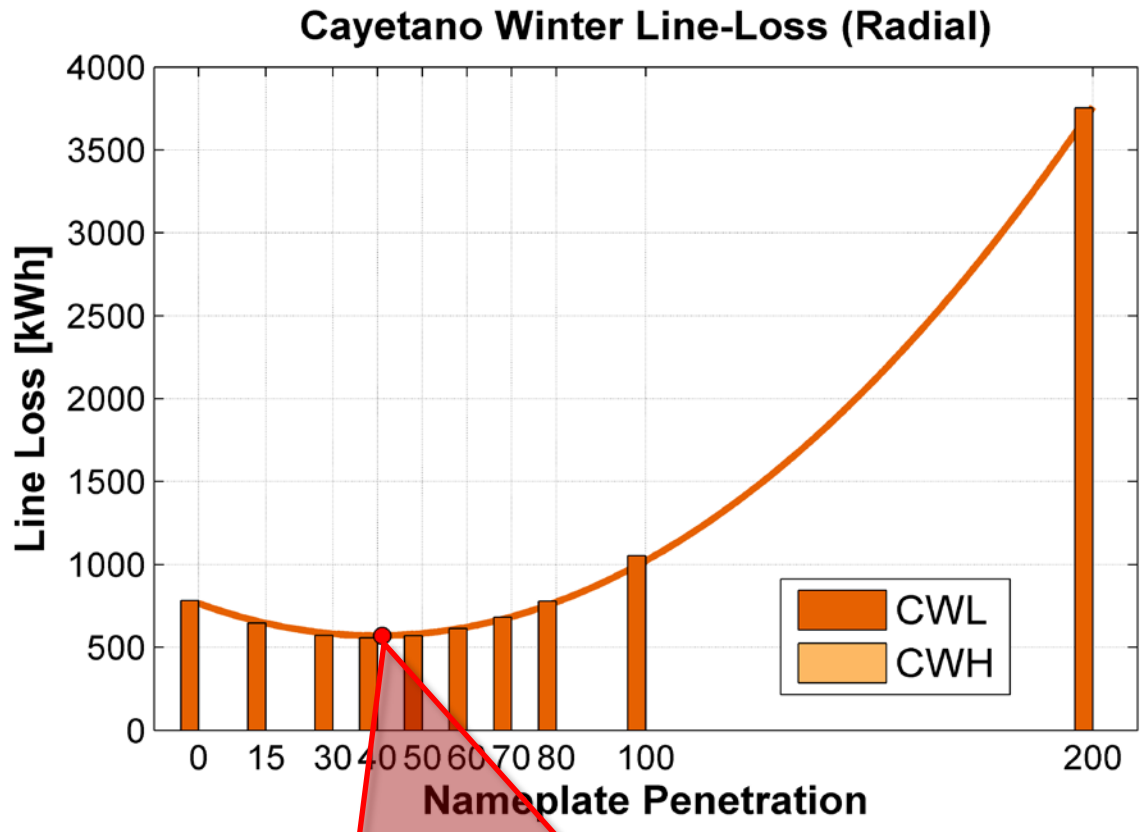
PV Generation is providing local demand support

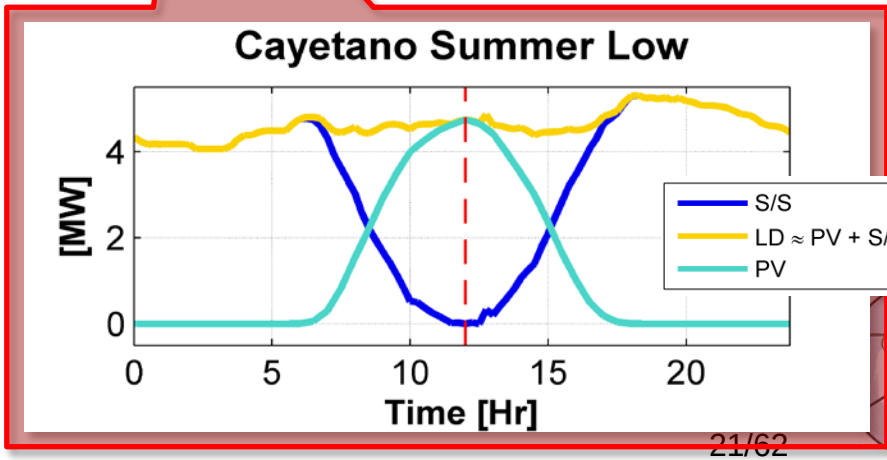
- As Penetrations increase, S/S current draw decreases

I^2R Line loss has quadratic dependence on penetration

Minimum at "Break Even Point"

- Depends upon daily demand





Task 3 Line Loss

PV Generation is providing local demand support

- As Penetrations increase, S/S current draw decreases

I^2R Line loss has quadratic dependence on penetration

Minimum at "Break Even Point"

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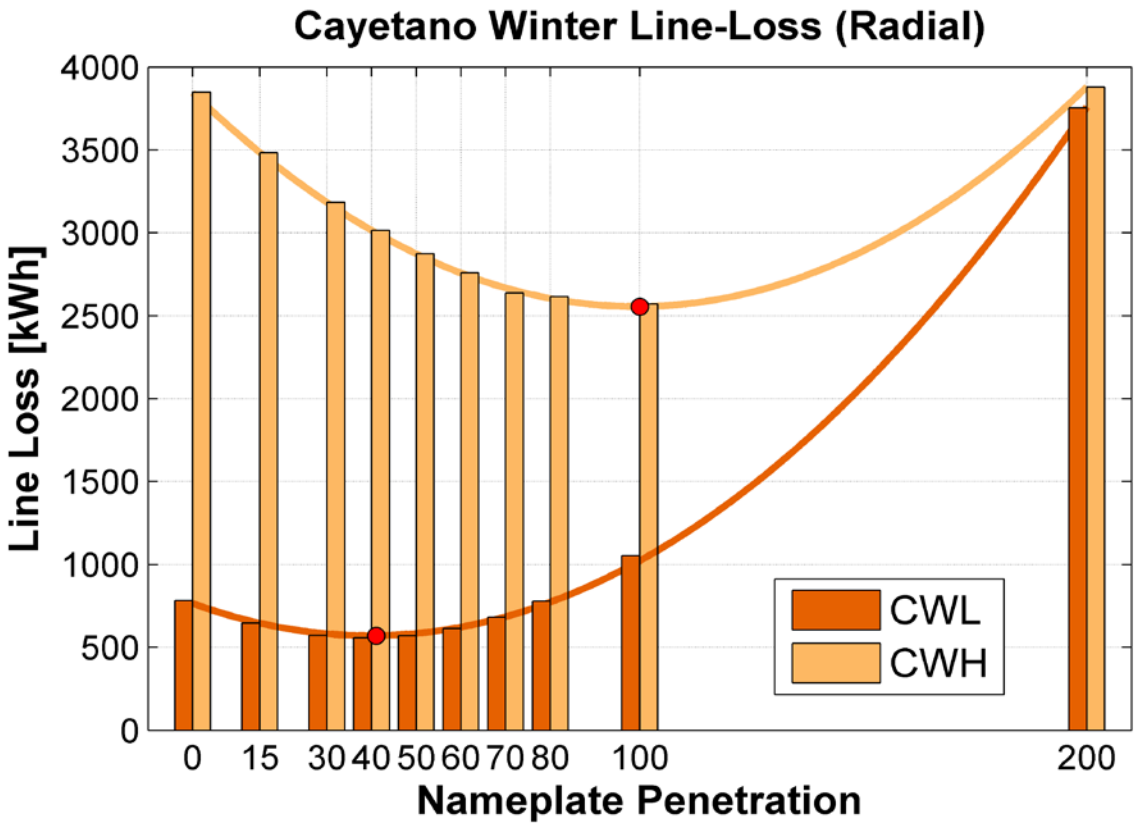
Interpolate to estimate optimum penetration (in terms of line loss)



Cayetano → 61% PV Penetration

Menlo → 56% PV Penetration

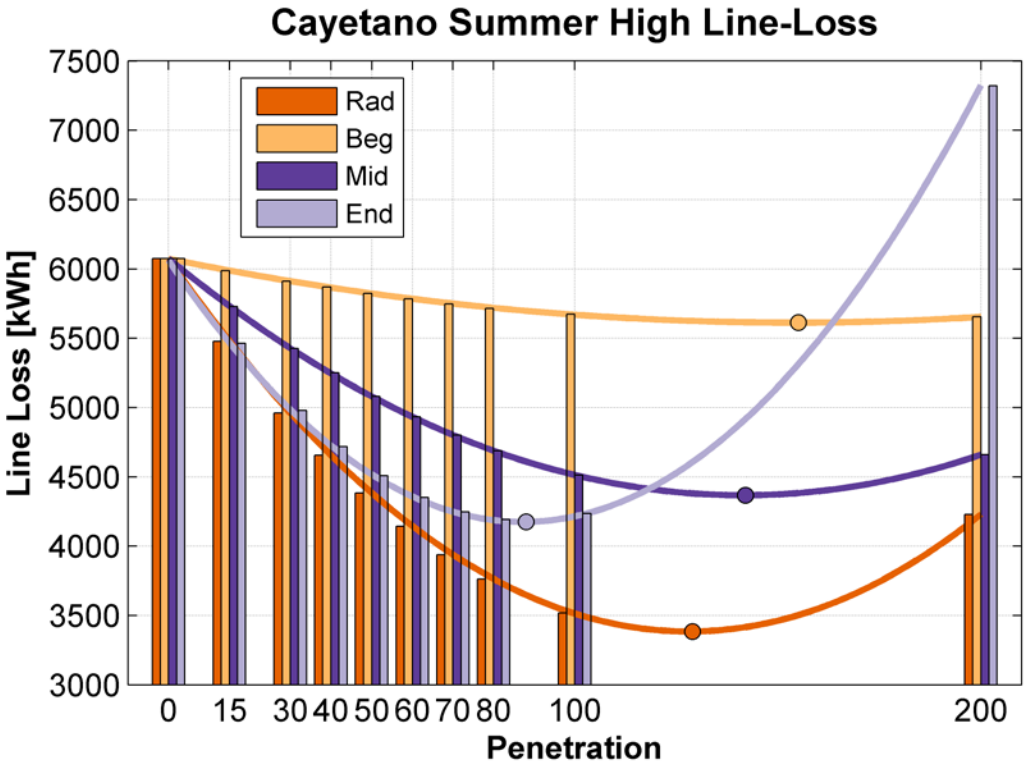
Task 3: System Losses

The optimal penetration point is also influenced by the distribution of the PV generation.

Radial distribution demonstrates the lowest loss at optimal penetration.

- Distributed nature of generation allows less excess generation

Point distributions have lower line loss at optimal penetration when $^{LC}/_{GC} \rightarrow 1$



Circuit	Distribution	LC/GC	Optimal %	Loss at Optimal %
Cayetano (LC = 0.85)	Radial	0.9	62	0.88 MWh
	Beginning	6.54	76	1.16 MWh
	Middle	1.6	68	1 MWh
	End	0.85	41	0.99 MWh
Menlo (LC = 0.42)	Radial	0.89	57	0.13 MWh
	Beginning	5.25	56	0.21 MWh
	Middle	0.95	48	0.15 MWh

Task 3 Quantify PV integration limits: Summary

Load Drop Compensation (at Sub-Station)

- Total LTC operations increase with increasing penetration
- LDC can mitigate high voltage conditions for end generation distributions (LC/GC<1)
- LDC can exacerbate low voltage conditions for beginning generation distributions (LC/GC>1

Minimal impact to Capacitor switching operation.

Buses with excess PV penetration downstream of the load demand and high line impedance are likely to produce high voltage conditions

- The proposed siting criteria can be used to mitigate high voltage conditions

Decrease in Power Factor on Low Demand days during PV generation as PV penetration increase.

Increased Levels of PV penetration will decrease line loss until Break Even Point penetration

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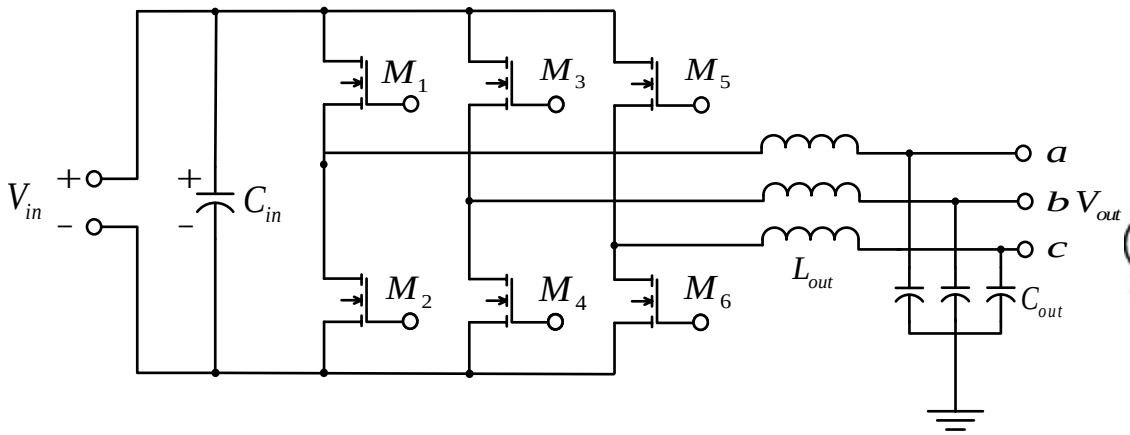
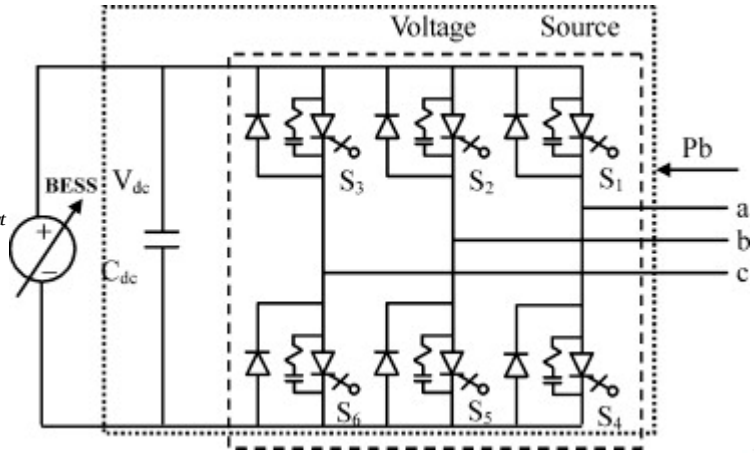
Task 4 Advanced Inverter Control

Assess the risks and benefits of advanced inverter control

- Advanced Inverter Controls
  - Volt/VAR Control
  - Active Power Filter
- Inverter Model Development
  - Model development
  - Single phase small scale DG (0-10kVA)
  - Three phase medium / large scale DG (+10kVA)



Inverter



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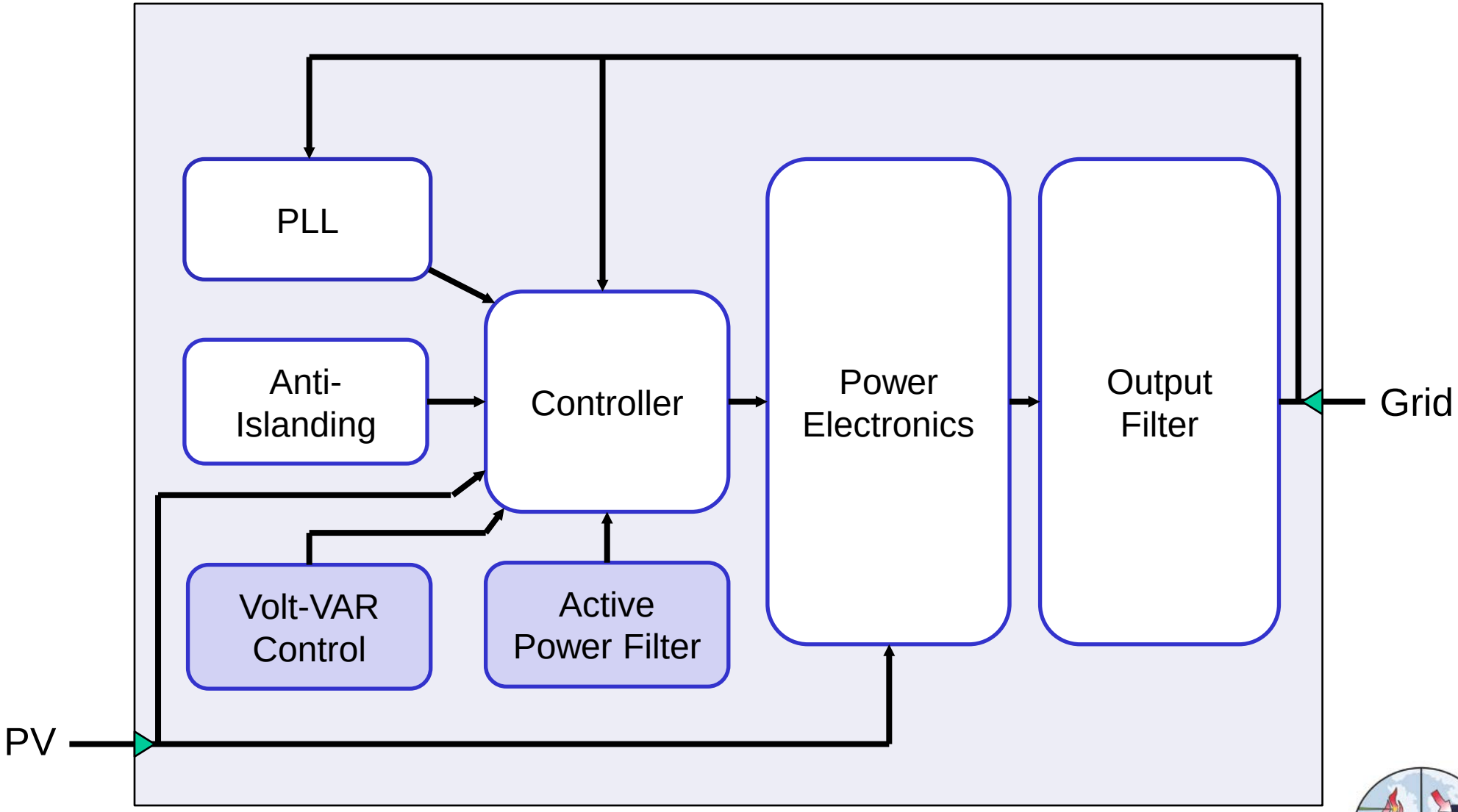
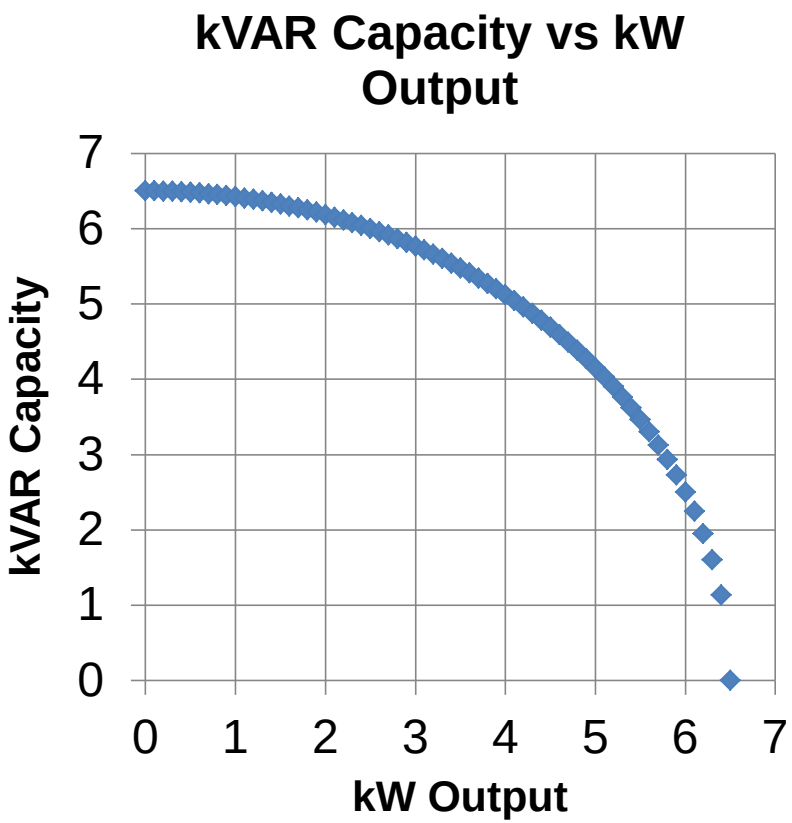
Task 4 Advanced Inverter Control

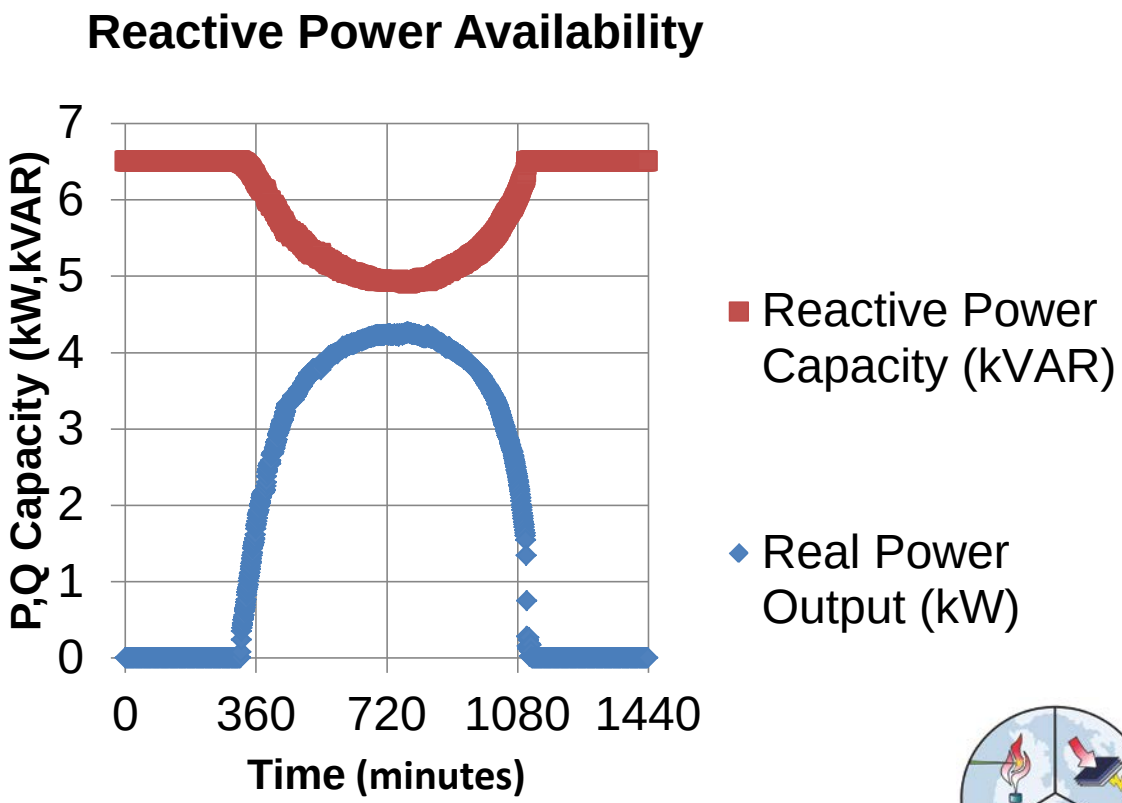


Task 4 Advanced Inverter Control - VVC

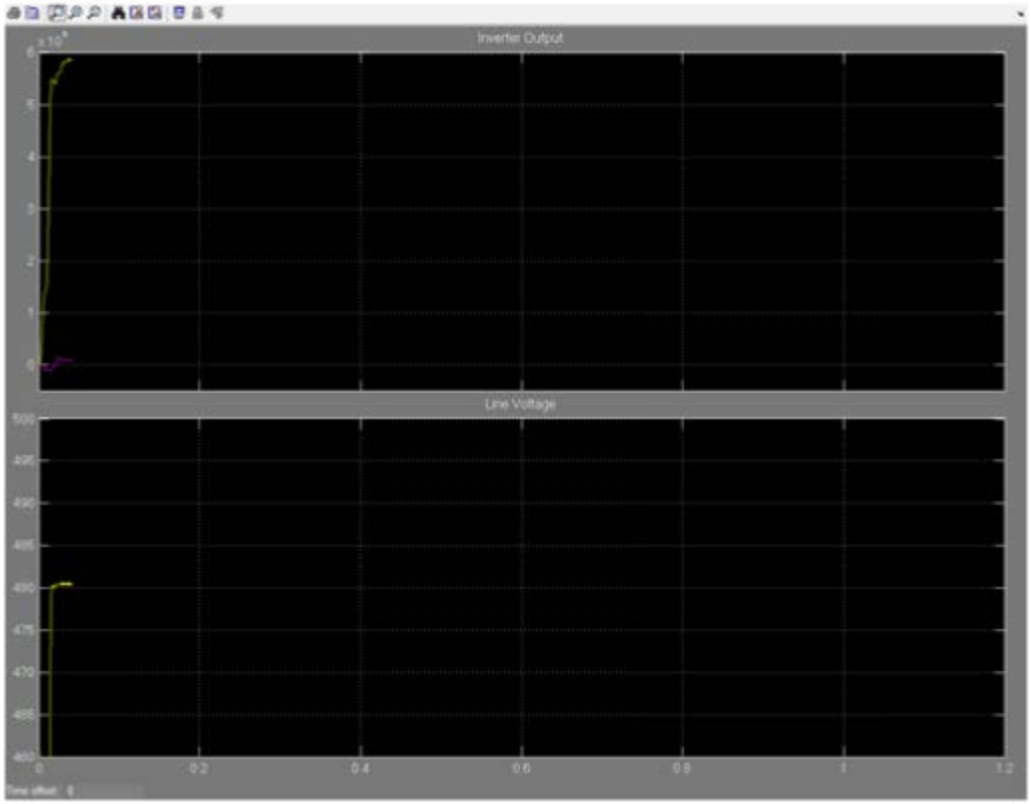
Volt – VAR control

- Utilize spare inverter capacity to provide reactive power support
- Utilize spare inverter capacity to provide local voltage regulation
- IEEE 1547 / IEEE 1547.8



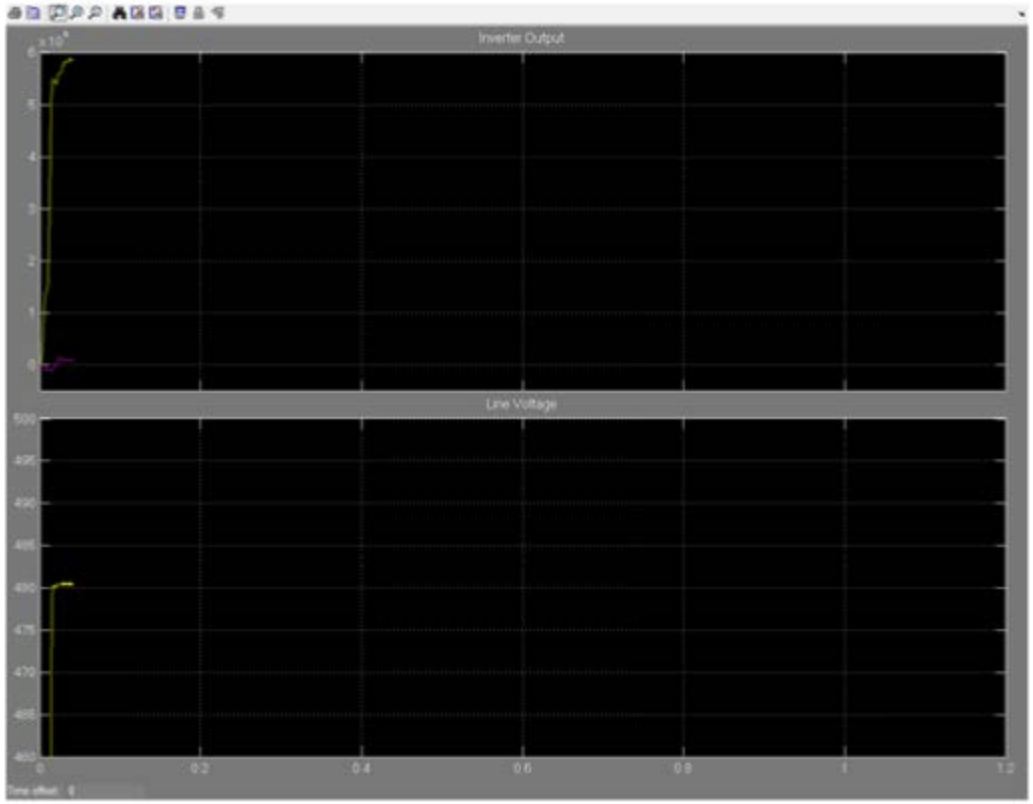


Task 4 Volt/VAR Control



- Real Power
- Reactive Power
- Line Voltage

Task 4 Volt/VAR Control



- Real Power
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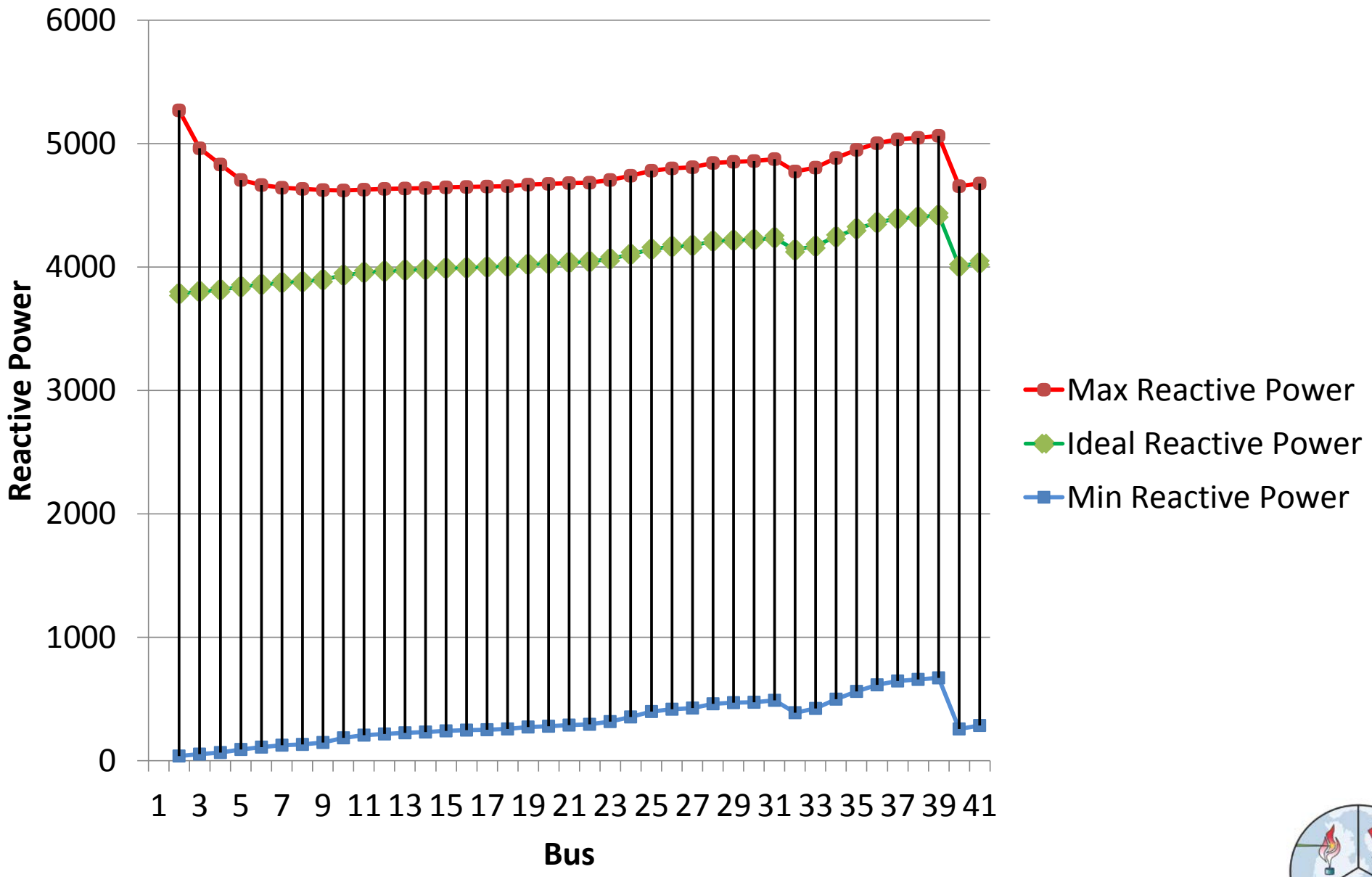
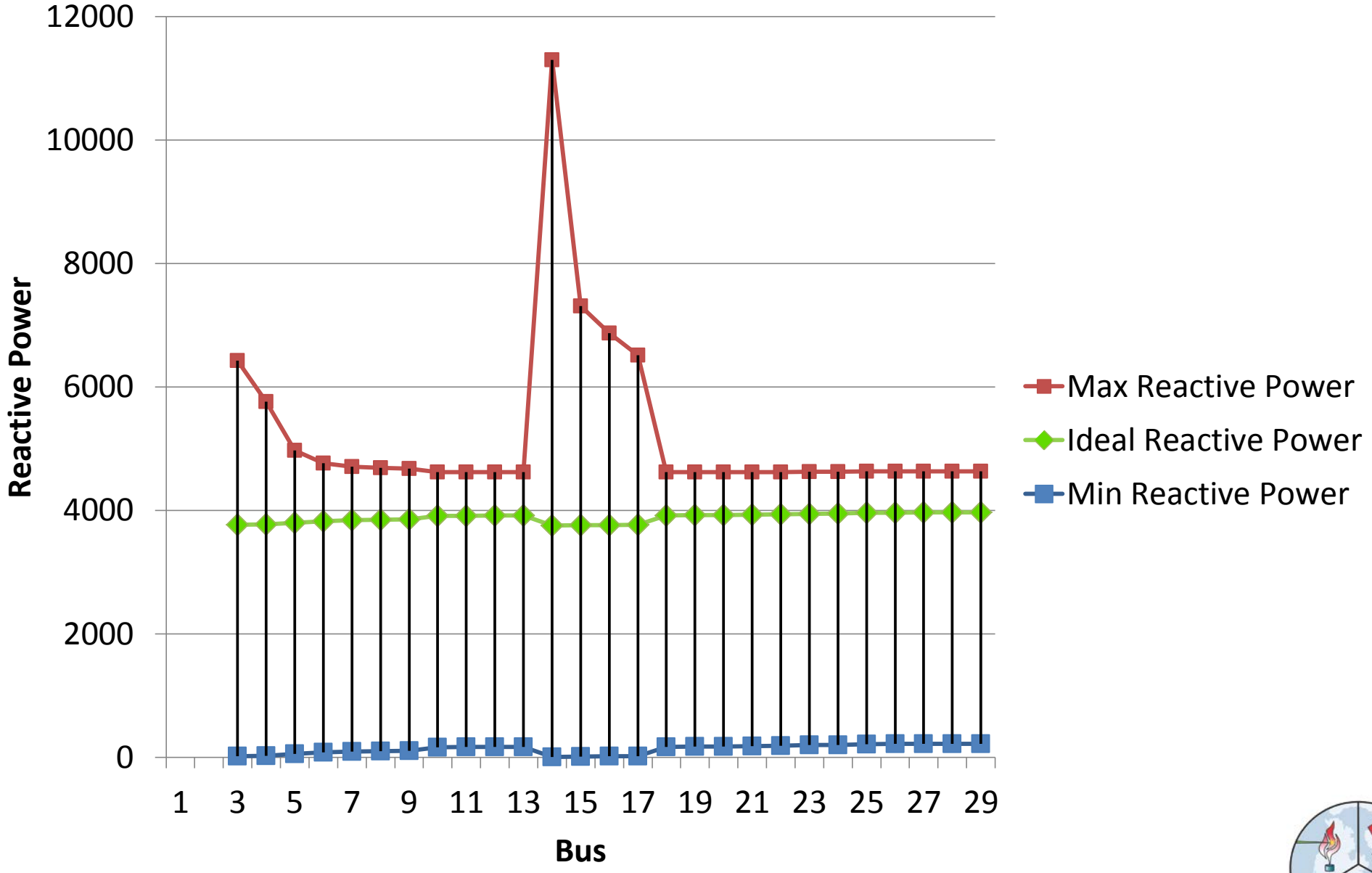
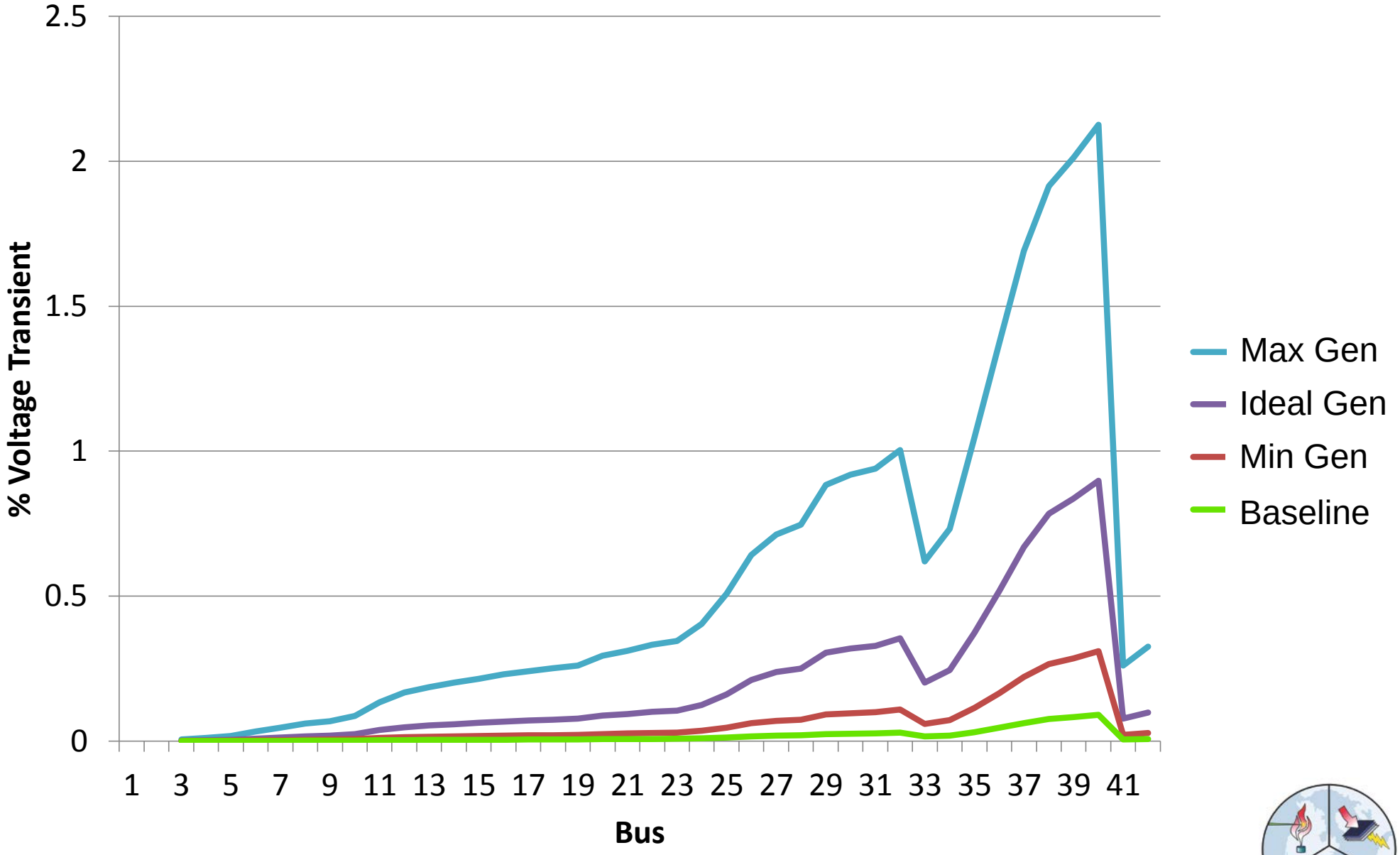
Task 4 Volt/VAR Menlo Limits



Task 4 Volt/VAR Cayatano Limits



Task 4 Volt/VAR Menlo Transient Results



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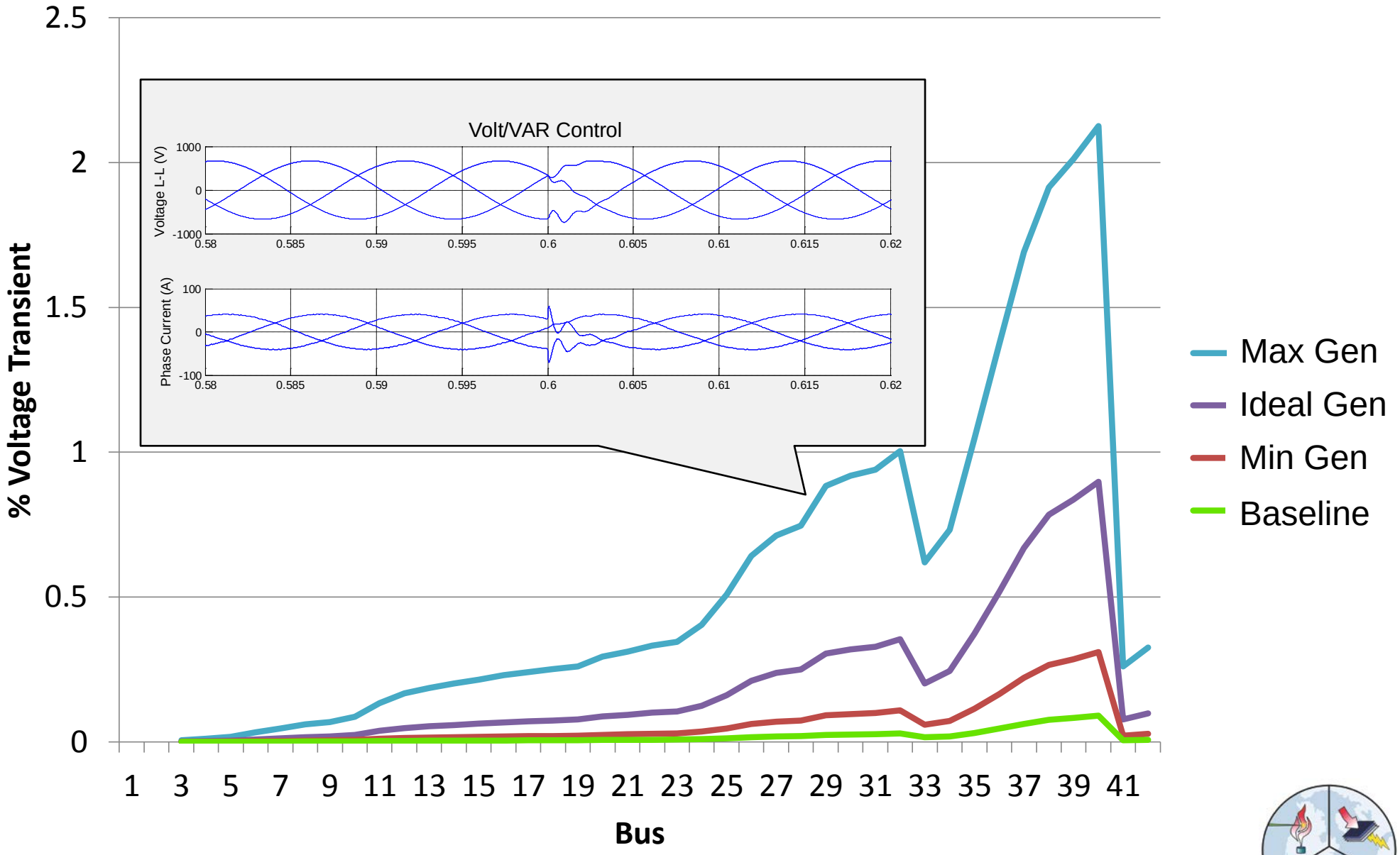
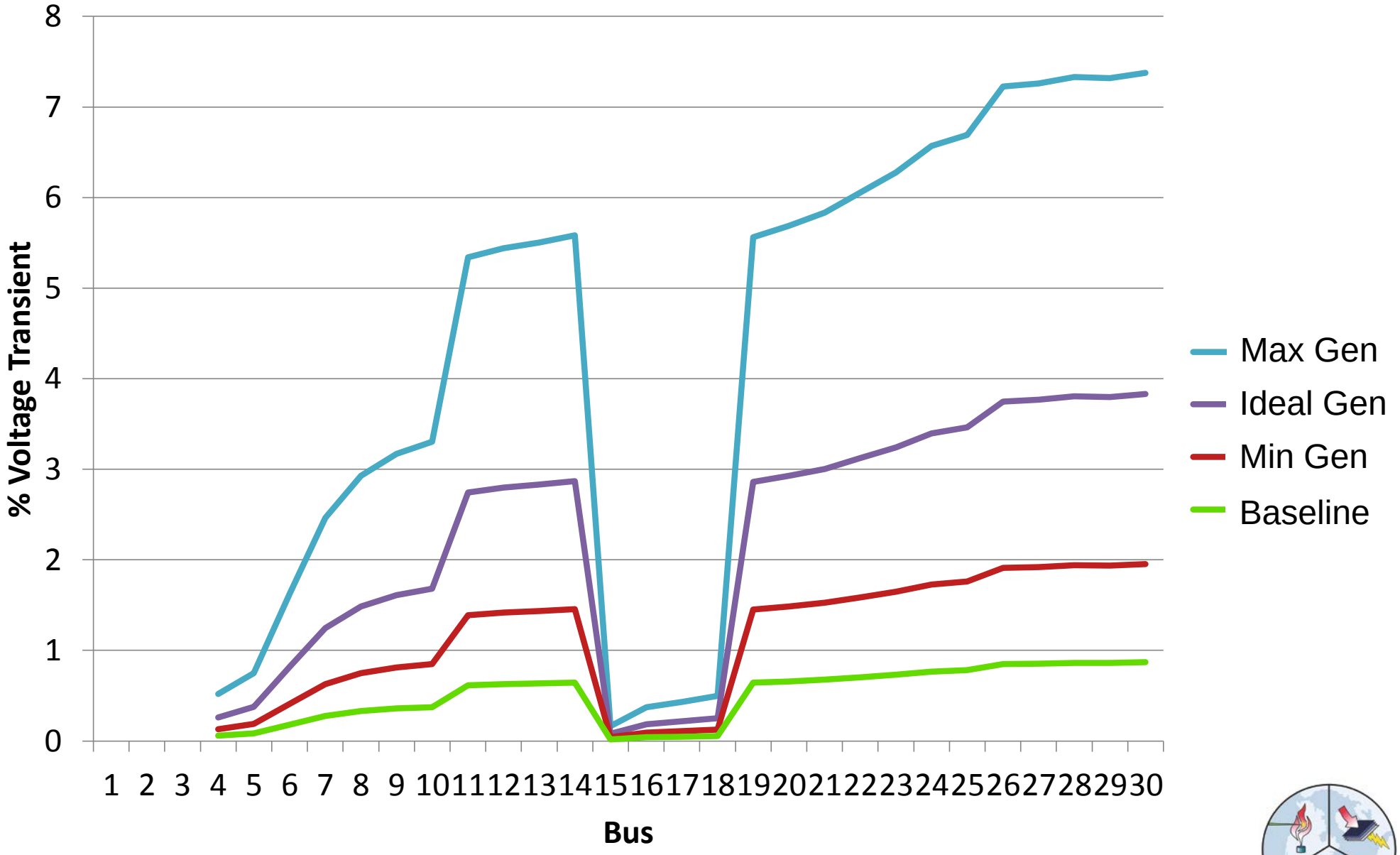


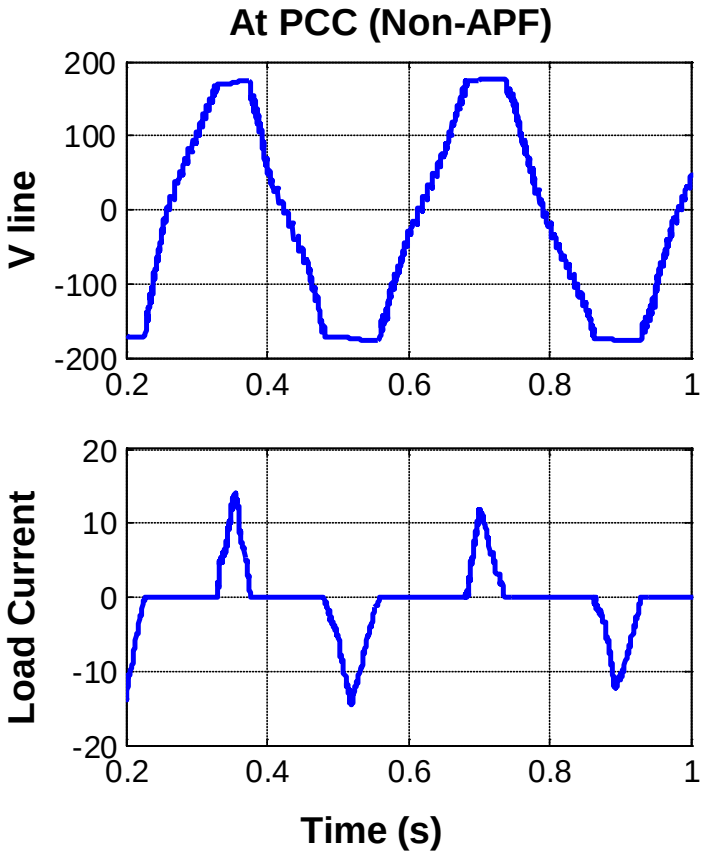
Task 4 Volt/VAR Cayatano Transient Results

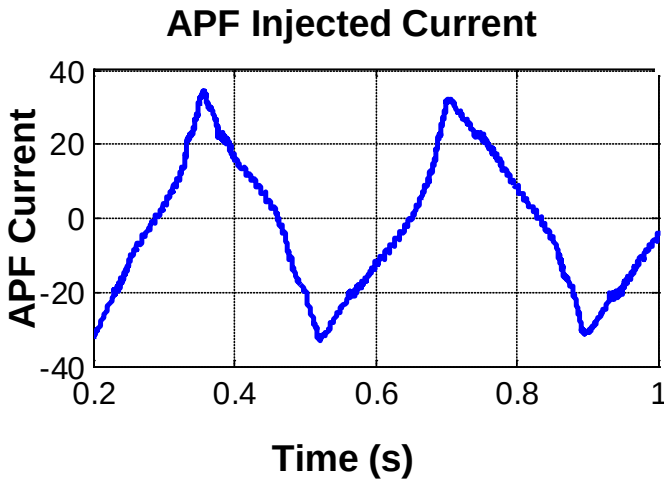


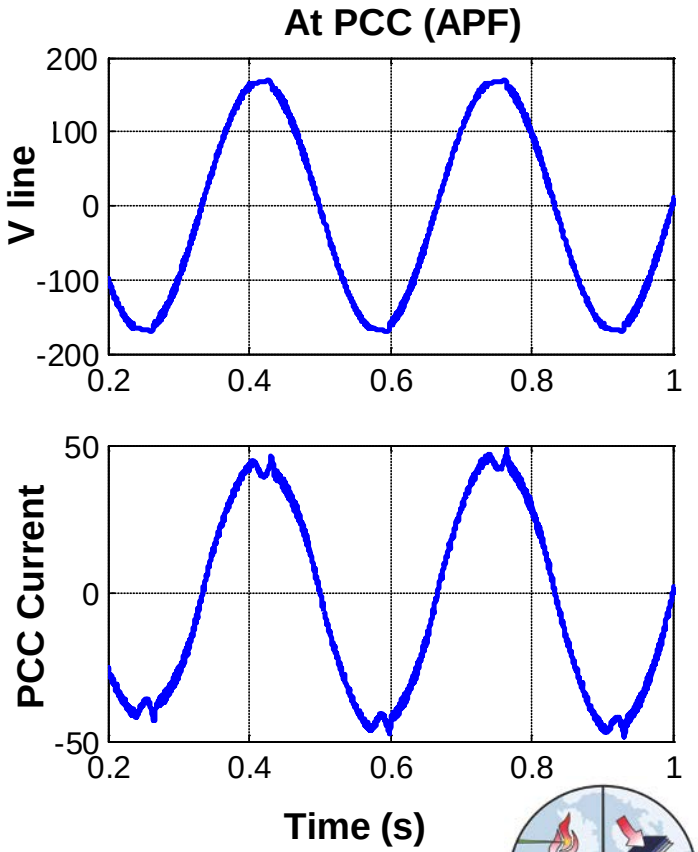
Task 4 Active Power Filter (APF)

Active Power Filter

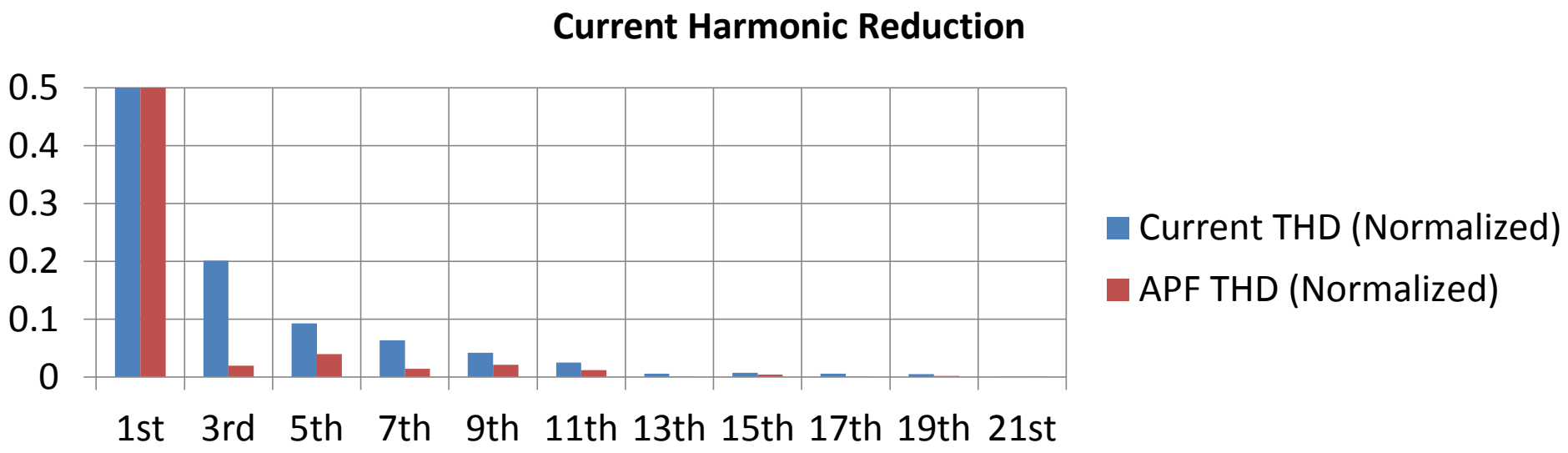
- Utilize inverter capacity to reduce harmonic distortion
  - Compensates nonlinear loads
  - Improves power quality, reduces flicker

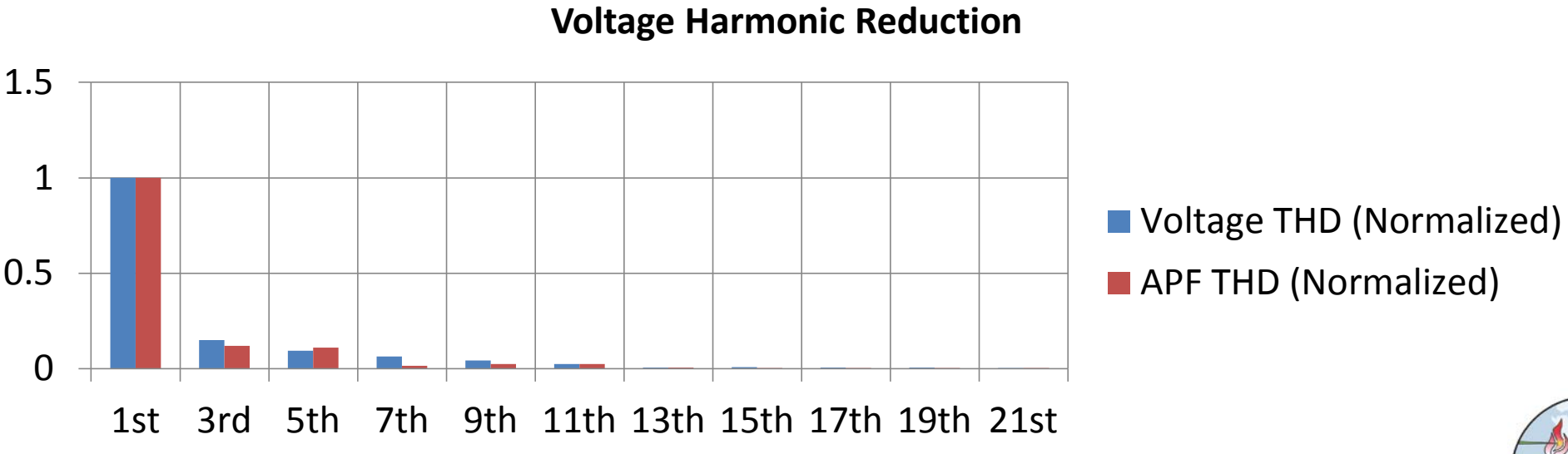






Task 4 Active Power Filter Results





Task 4 Summary

- Volt/VAR Control
  - May use spare capacity to provide reactive power support (D-STATCOM)
  - May increase line capacity
  - May reduce utility voltage control ability
  - May inject local voltage transients
  - Transient performance dependent on line impedance and load / generation conditions

- Active Power Filter (APF)
  - Remove harmonic distortion
  - Adds additional costs to customer

Advantage Potential Hazard

Tasks & Key Deliverables

Task 1 Project management

Task 2 Model development and evaluation

- Model scenarios and comparisons to grid monitored data

Task 3 Quantify PV integration limits

- Determine limits for PV penetration within existing circuit architectures and with existing technology

Task 4 Advanced inverter control

- Assess the risks and benefits of advanced inverter control

Task 5 Integrated distribution grid control

- Progressively introduce and assess smart integrated distribution technologies/ controls to determine impacts on PV penetration

Task 6 Practical feasibility and outreach

- Determine market potential of technology and encourage adoption

Task 5

Progressively introduce and assess smart integrated distribution technologies controls to determine impacts on PV penetration

Advanced Steps

- Advanced Inverter Controls
  - Volt/VAR Control
  - Active Power Filter

Progressive Steps

- High Voltage
  - Line Re-Conductor
  - Siting
- Low Voltage
  - System Voltage
  - Line Regulator
  - LDC Current Compensation
- Power Factor Sensitivity
  - VAR Switching

Task 5 High Voltage

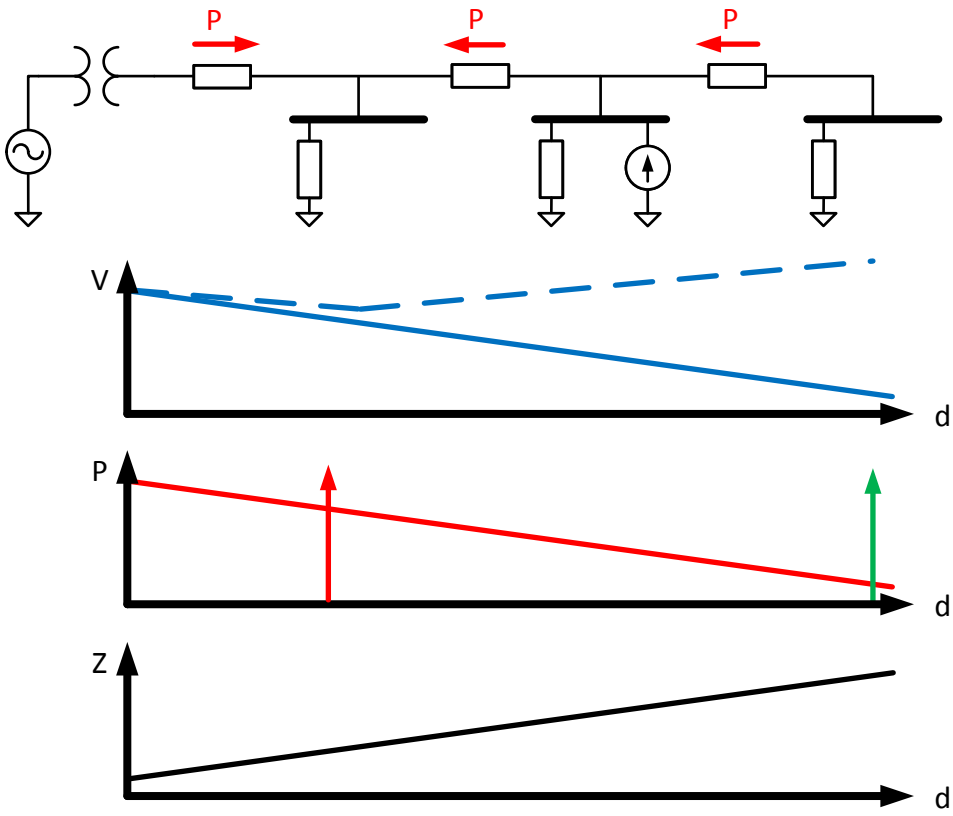
High Voltage occurs:

- Excessive generation at lower penetrations
- High impedance between GC and LC

Menlo End distributions featured high voltages for any increase PV penetration.

Possible Remedies:

- Re-conductor line
- Re-Site PV installation



Task 5 High Voltage: Re-conductor

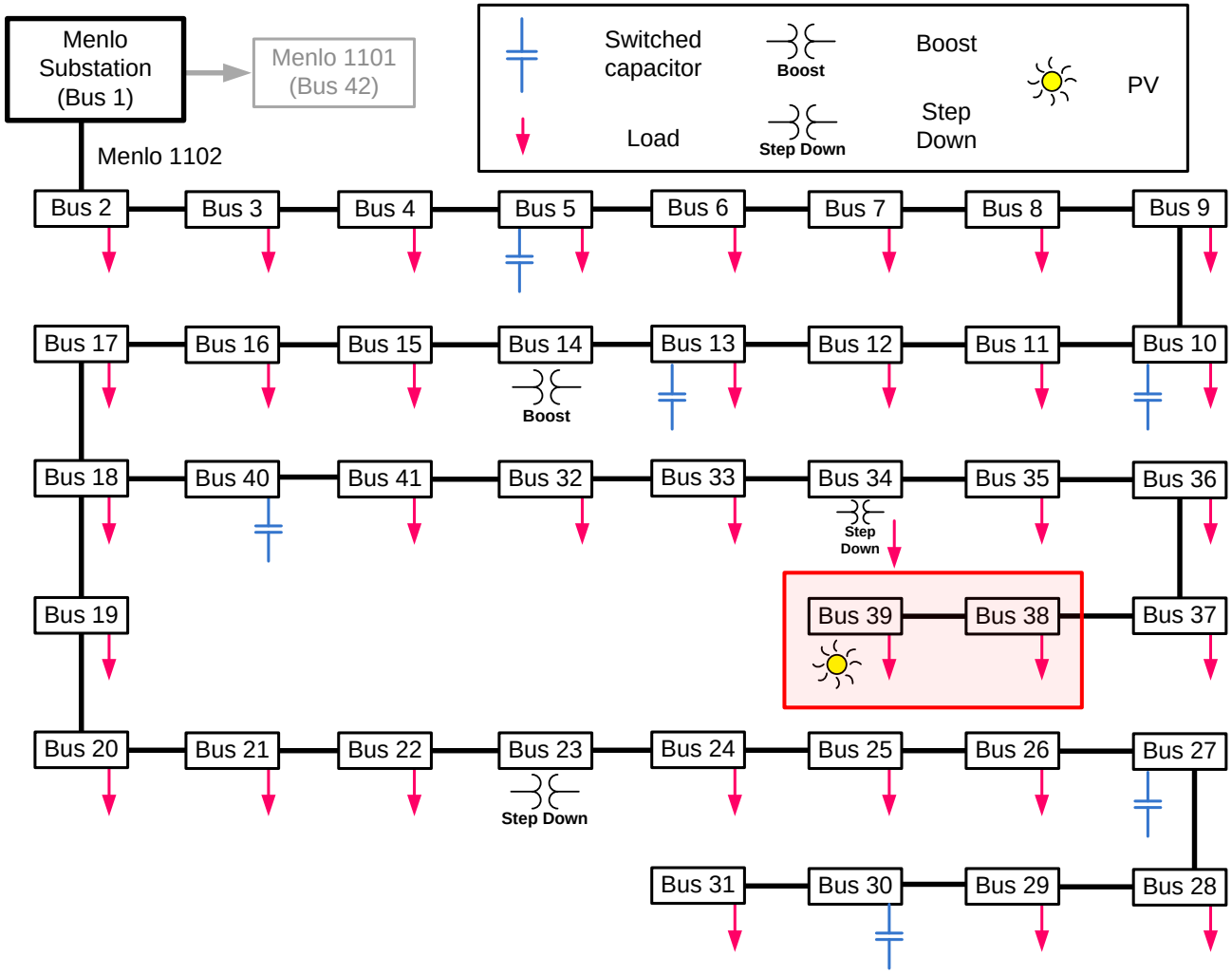
Re-conductored high impedance end section to assisted in High Voltage.

#4 ACSR

- 0.468 Ω/1000ft

1/0 Stranded Cu

- 0.117 Ω/1000ft

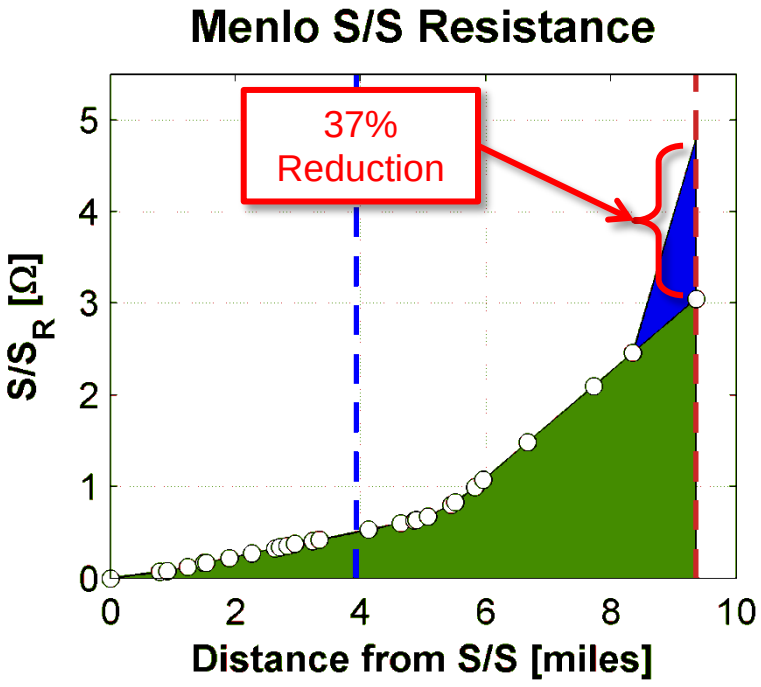


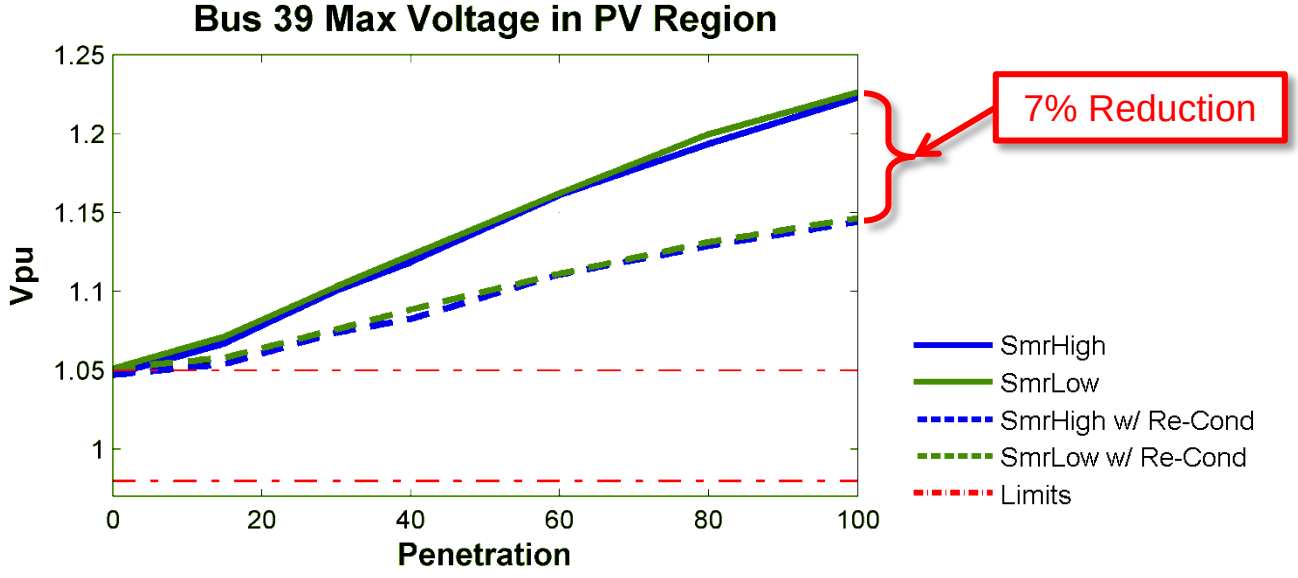
Task 5 High Voltage: Re-Conductor

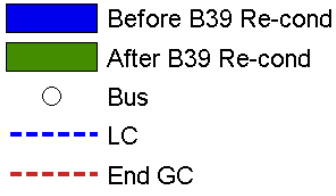
In this application, re-conductoring lowered voltage rise but not to standard bounds.

Generation on at bus 39 is prone to voltage rise even after re-conductoring:

- High Impedance to S/S (3Ω)
- Generation located away and downstream from load (LC/GC = 0.42)





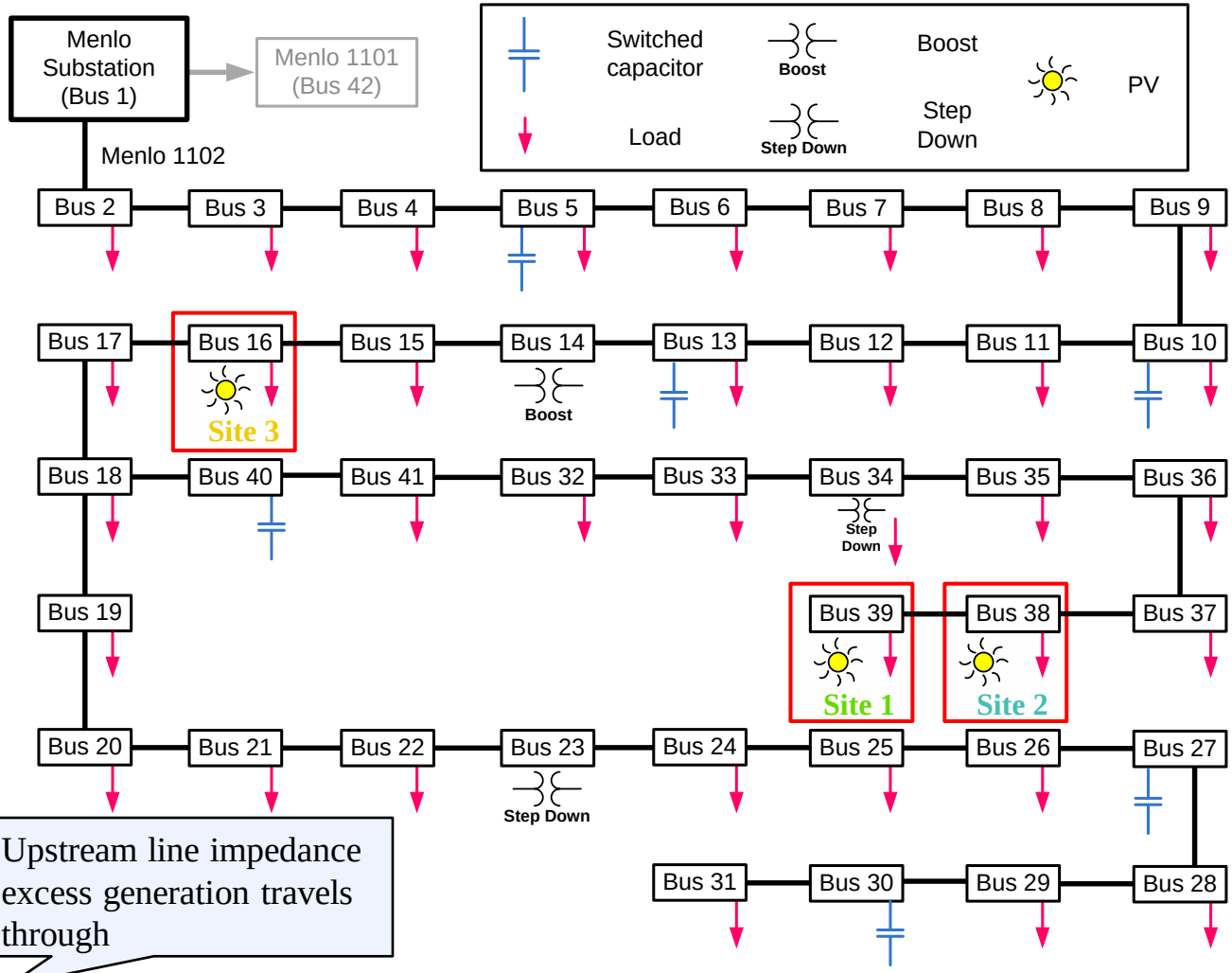


Task 5 High Voltage: Siting

Line Impedance and excess generation capacity significant impact voltage rise.

- Generation sites are more prone the DG induced voltage rise can be avoided

Voltage Rise Siting (VRS) combines characteristics of DG induce voltage rise into a score.



Break even penetration at bus

Upstream line impedance excess generation travels through

$$\mathbf{VRS} = \boldsymbol{RPF_{Pen}}(25\%) + \boldsymbol{RPF_{R}}(25\%) + \boldsymbol{RPF_{R0}}(25\%) + \boldsymbol{R_{S/S}}(25\%)$$

Line Impedance of DG bus

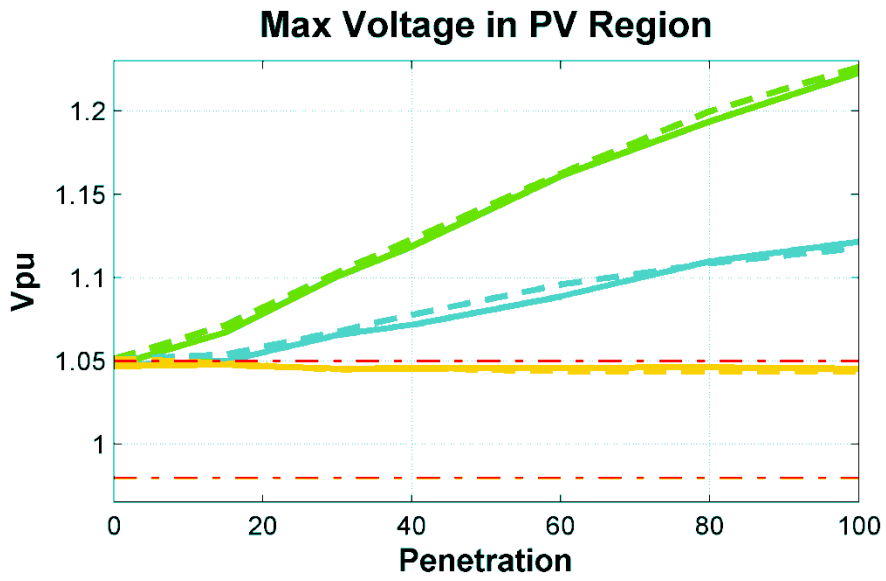
Line Impedance to sub-station

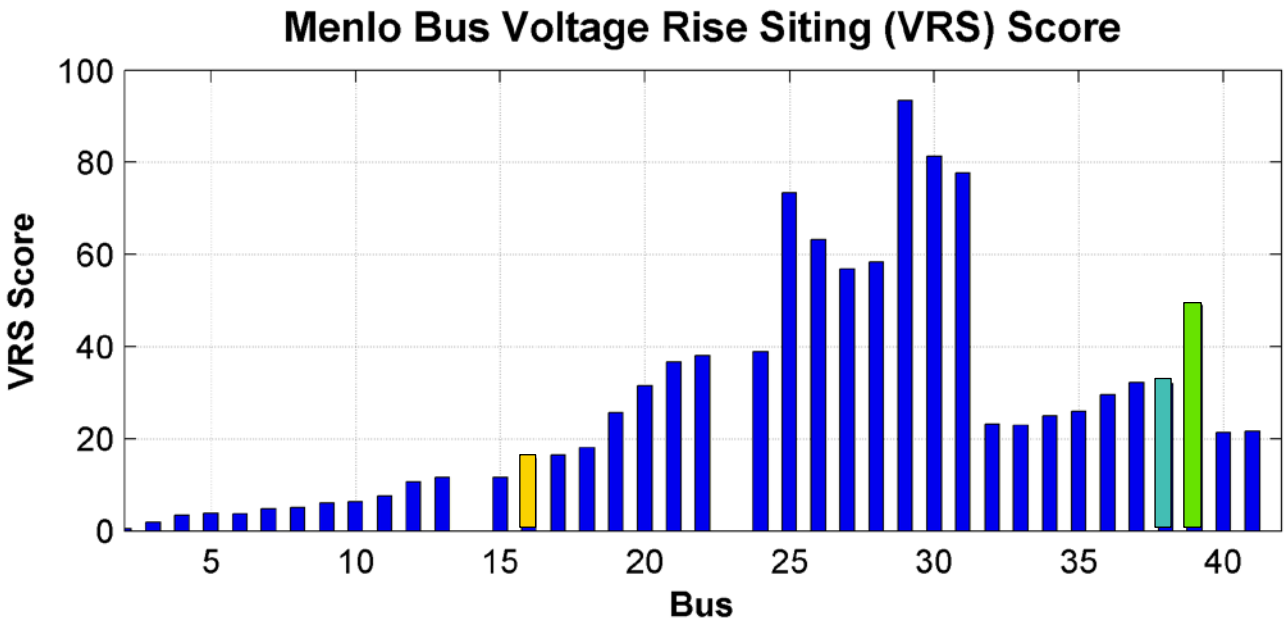
Task 5 High Voltage: Siting

A high VRS score indicates a site is prone to DG induced voltage rise.

- Site 1: VRS = 48.9
- Site 2: VRS = 31.9
- Site 3: VRS = 15.7

For the Menlo circuit, point generation sites should score less than equal to Site 3.





Site 1: SmrHigh
Site 1: SmrLow
Site 2: SmrHigh
Site 2: SmrLow
Site 3: SmrHigh
Site 3: SmrLow
Limits

Task 5 Low Voltage

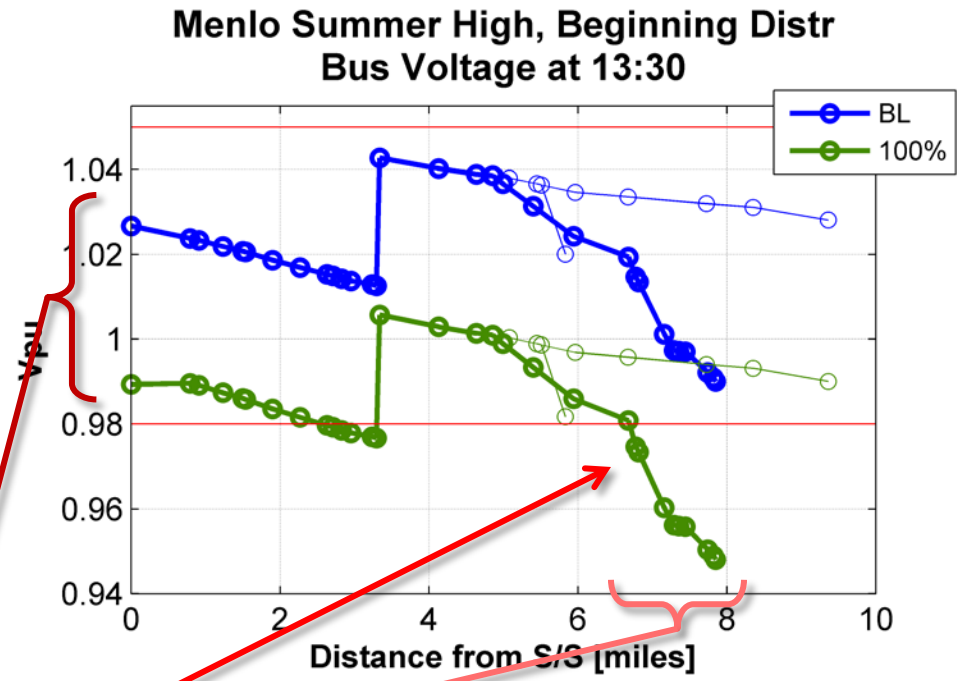
Low Voltage occurs (with LDC):

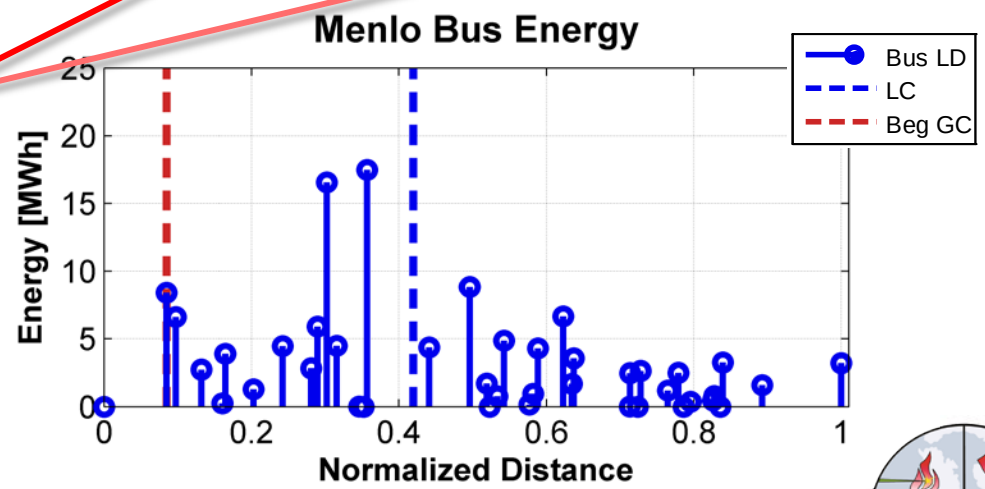
- LC is behind GC ($\frac{LC}{GC} \geq 1$)
- High Penetrations of PV generation

High Levels of PV Generation cause LDC to tap down, causing a Low Voltage conditions at peak PV generation.

Possible Remedies:

- Raise System voltage
- Line Regulator
- LDC Current Compensation





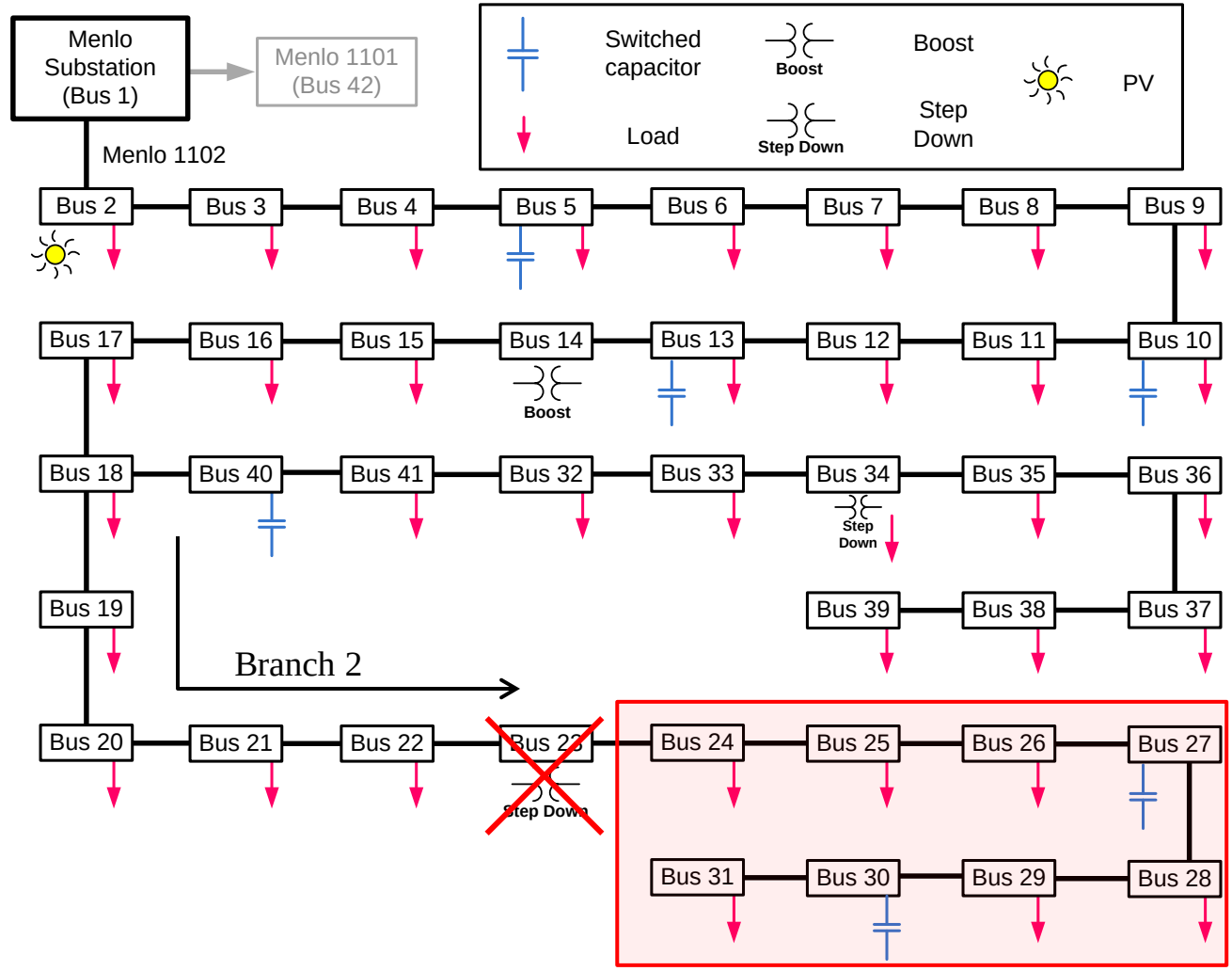
Task 5 Low Voltage: System Voltage

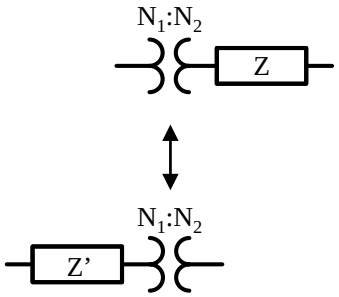
The Menlo circuit supports a 4.16kV section at the end of the circuit.

For the same load demand, lower voltages draw more current over the same line impedance.

- More voltage drop

Raising Voltage to 12.47kV will reduce equivalent impedance by a factor of 9.





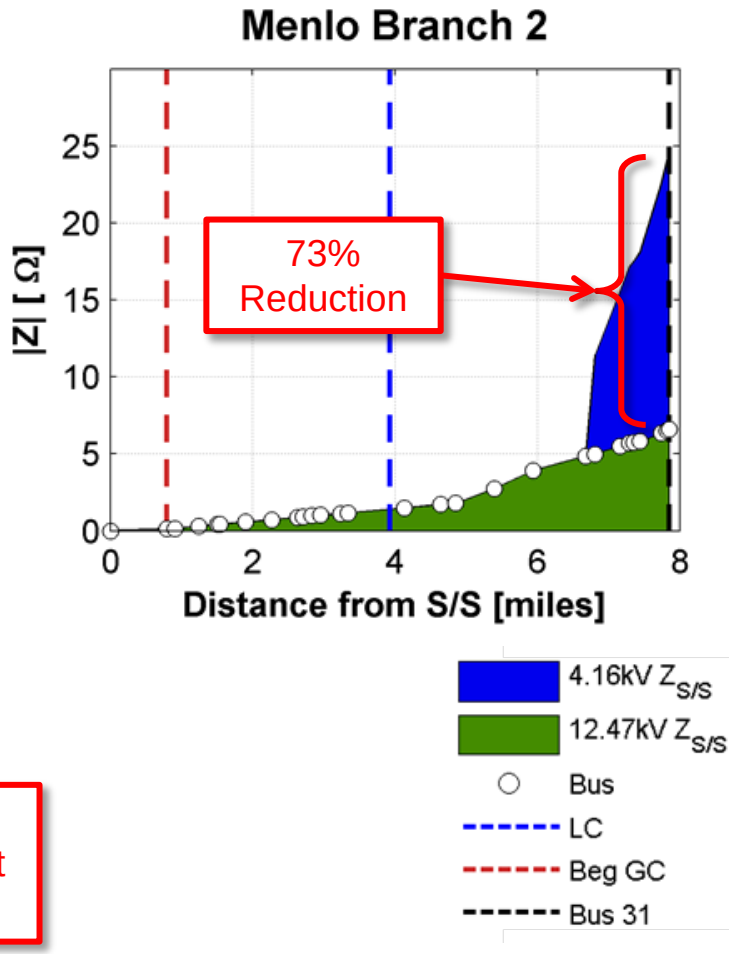
$$Z'_{12.47kV} = \left(\frac{N_1}{N_2}\right)^2 \cdot Z_{4.16kV}$$

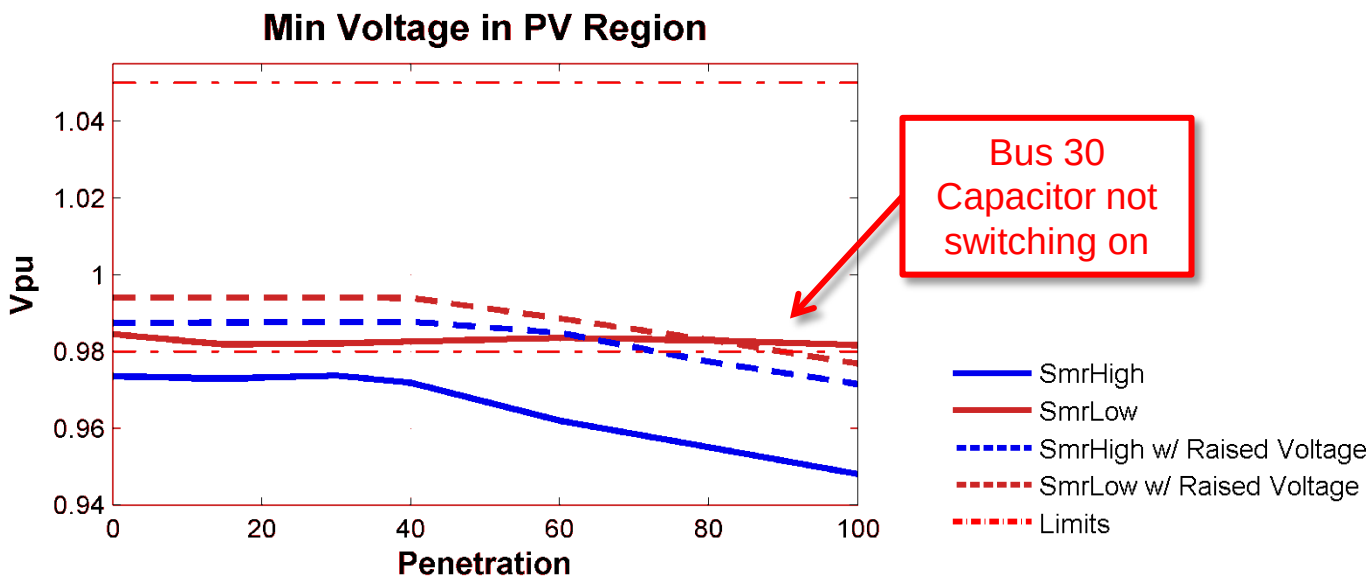
Task 5 Low Voltage: System Voltage

Raising system voltage for 4.16kV section to 12.47kV decreased the amount of the voltage drop at end of Menlo's branch 2.

PV penetration limit extended from 40% to 100% for Menlo Beginning scenario.

- 0.97pu is considered marginal.





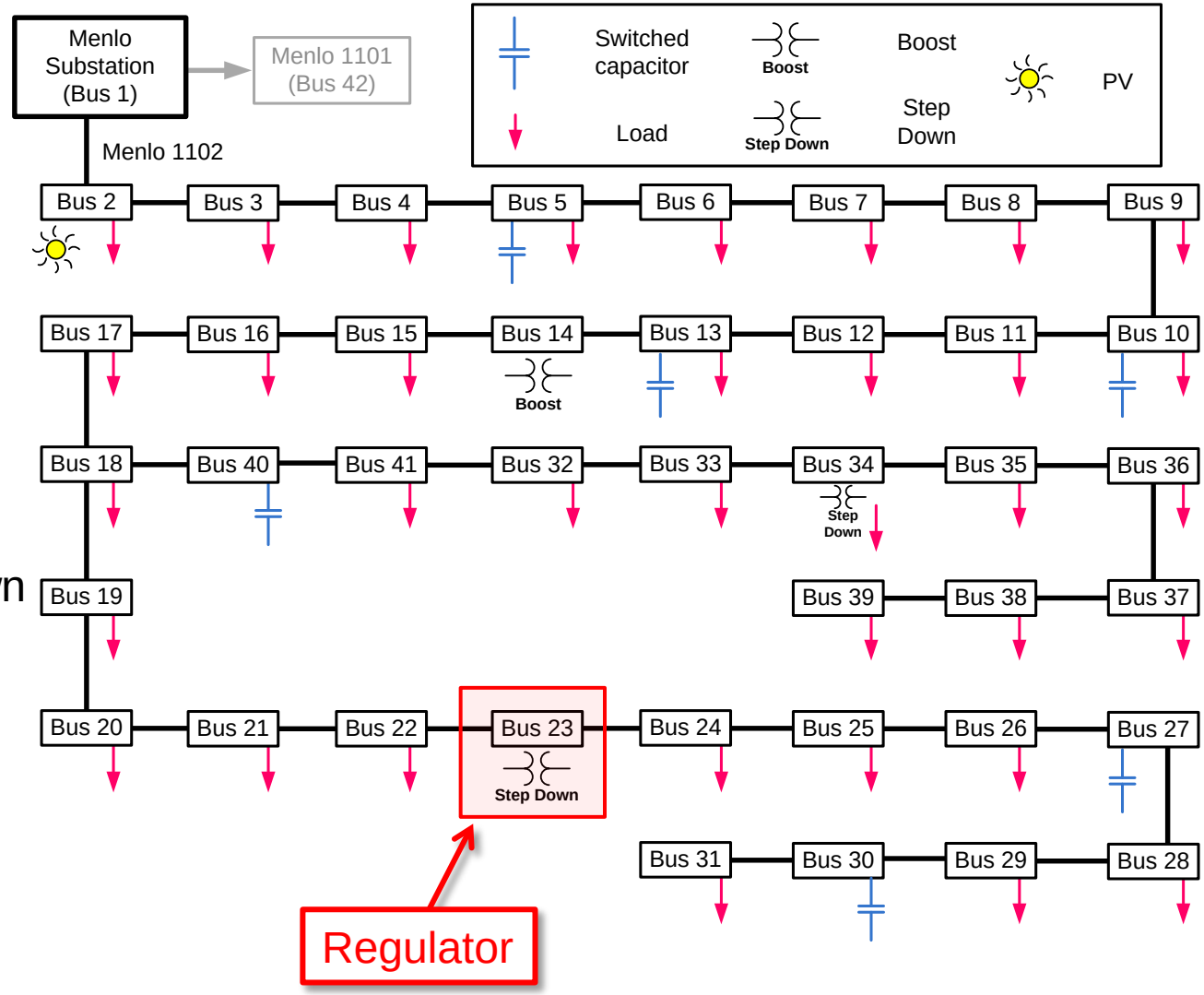
Task 5 Low Voltage: Line Regulator

Low Voltage condition is occurring at the end of the circuit

- Place a Line Regulator

Line Regulators use the same controls as the OLTC w/ LDC

- High current → Tap up
- Low current → Tap down



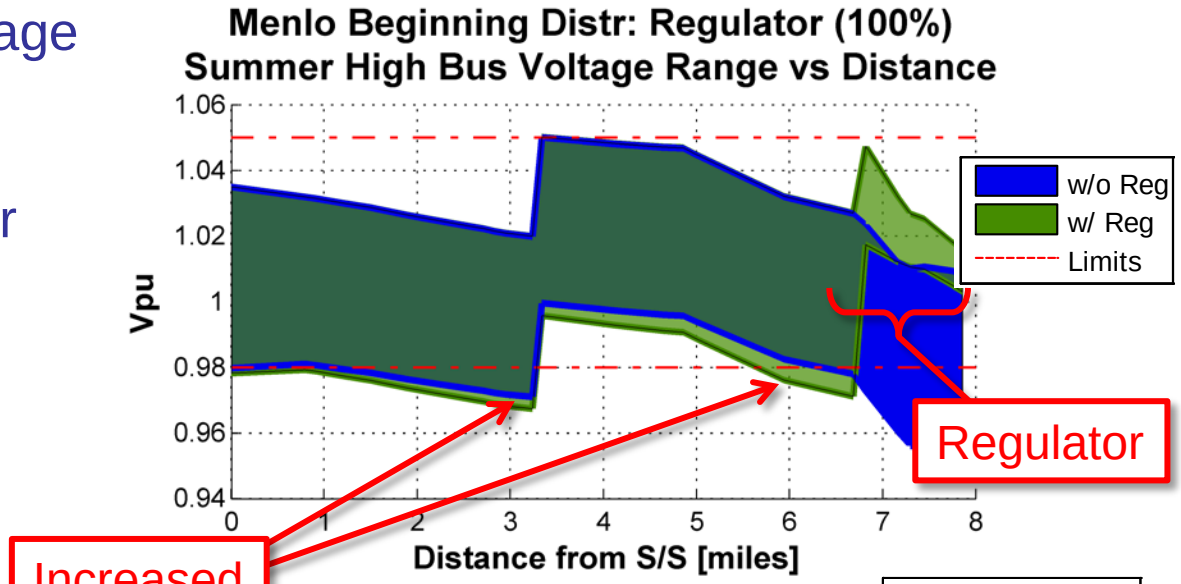
Task 5 Low Voltage: Line Regulator

Line Regulator maintains low voltage section in standard bounds.

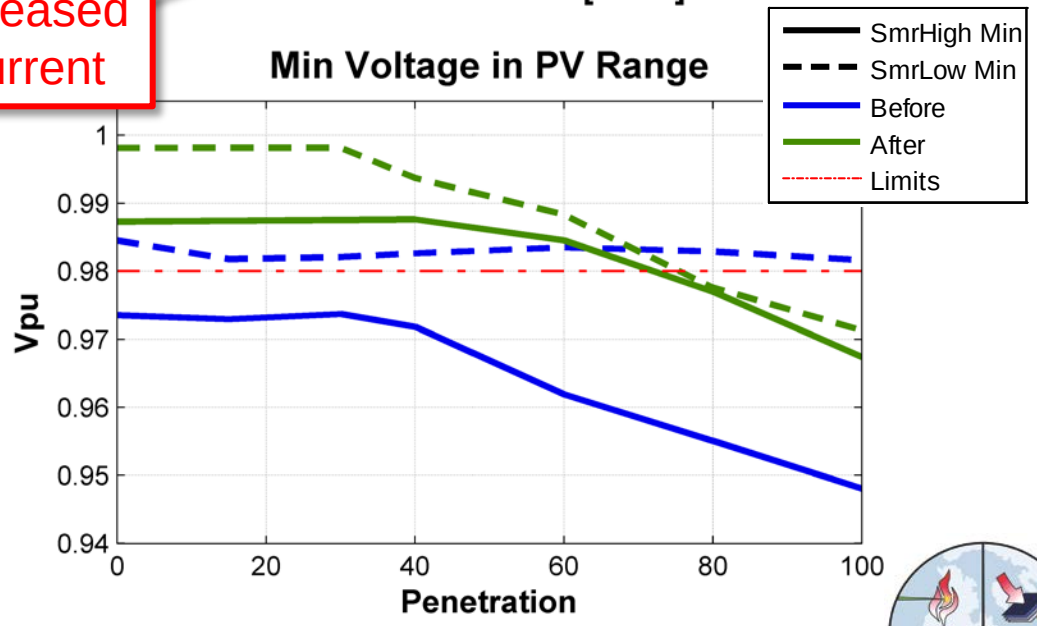
Improved low voltage condition for penetrations up to 70% on Menlo.

Beyond 70%, the bus voltage upstream of regulator is in Low Voltage condition

- Condition aggravated by incre current caused by Regulator.



Increased Current



Task 5 Low Voltage: LDC Current Compensation

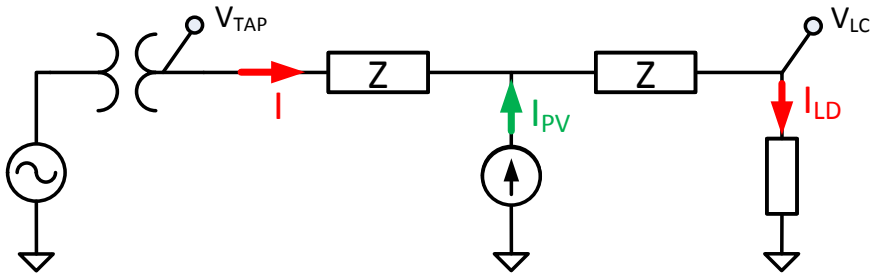
High Levels of PV Generation cause LDC to tap down, causing a Low Voltage condition at peak PV generation.

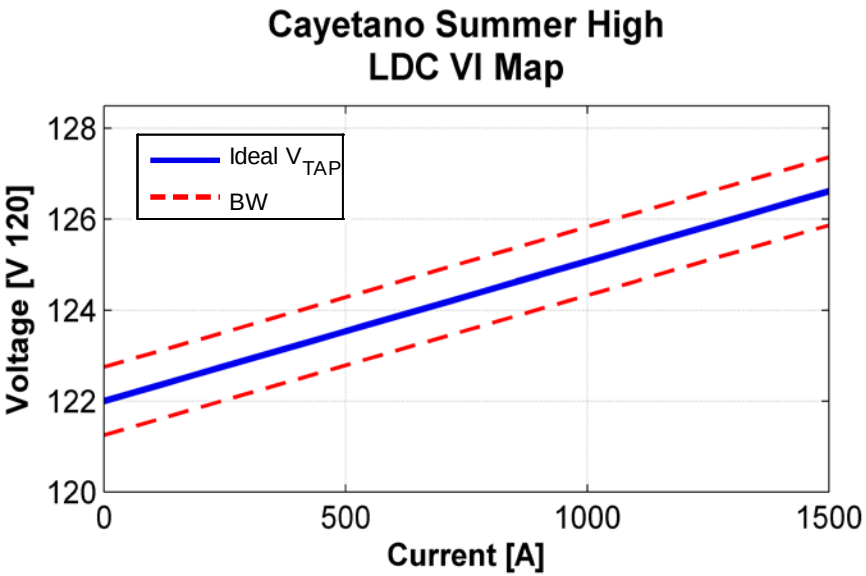
- Load behind Generation ($\frac{LC}{GC} \geq 1$)

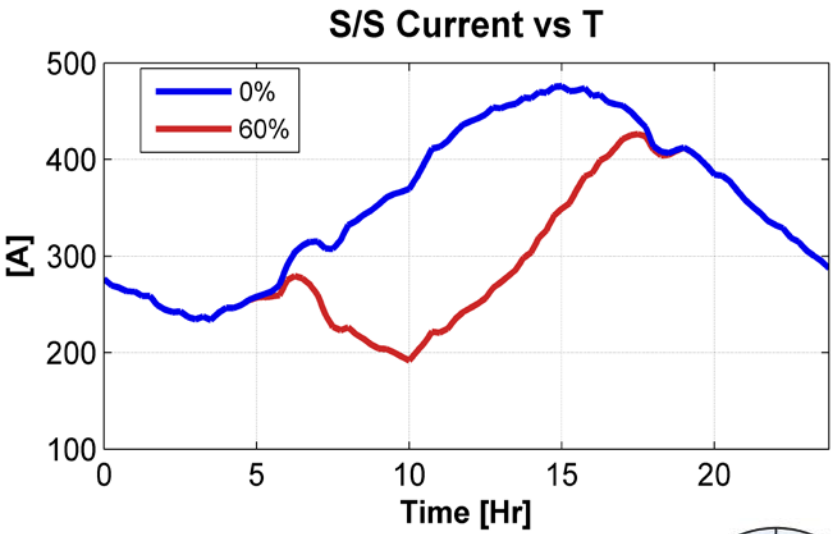
LDC controls use S/S current to estimate the ideal voltage set point of the OLTC.

$$I \propto V_{TAP}$$

$$I = I_{LD} - I_{PV}$$







Task 5: Low Voltage - LDC Current Compensation

High Levels of PV Generation cause LDC tap down, causing a Low Voltage conditior at peak PV generation.

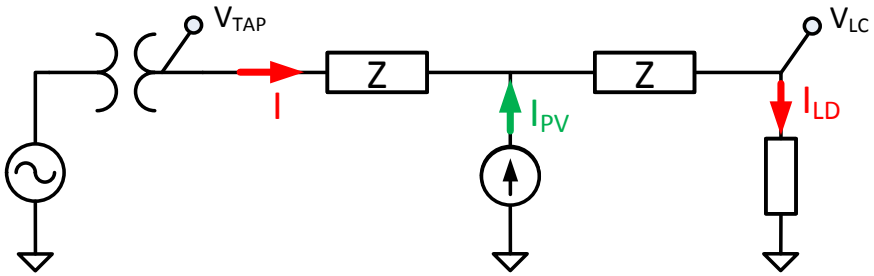
- Load behind Generation ($\frac{LC}{GC} \geq 1$)

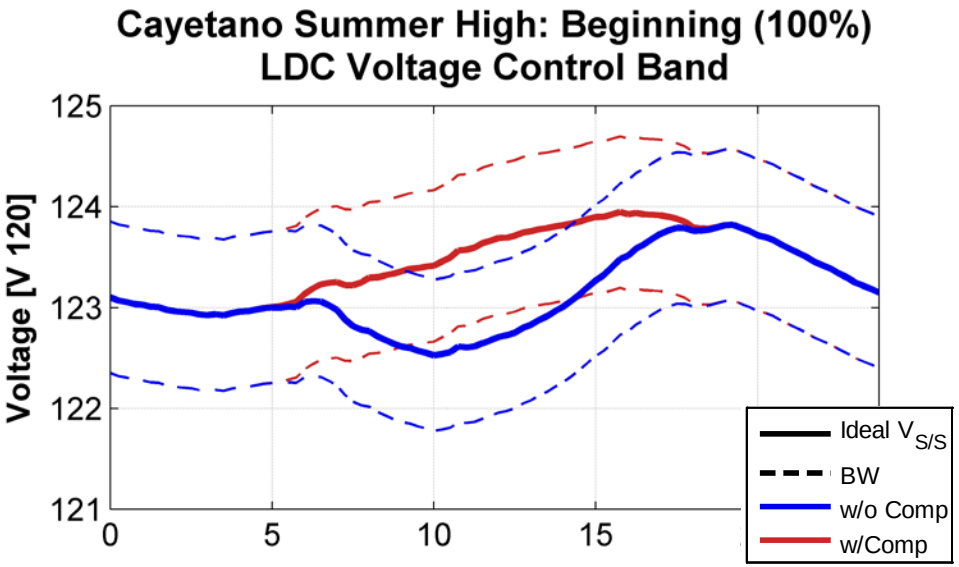
LDC controls use S/S current to estimate the ideal voltage set point of the OLTC.

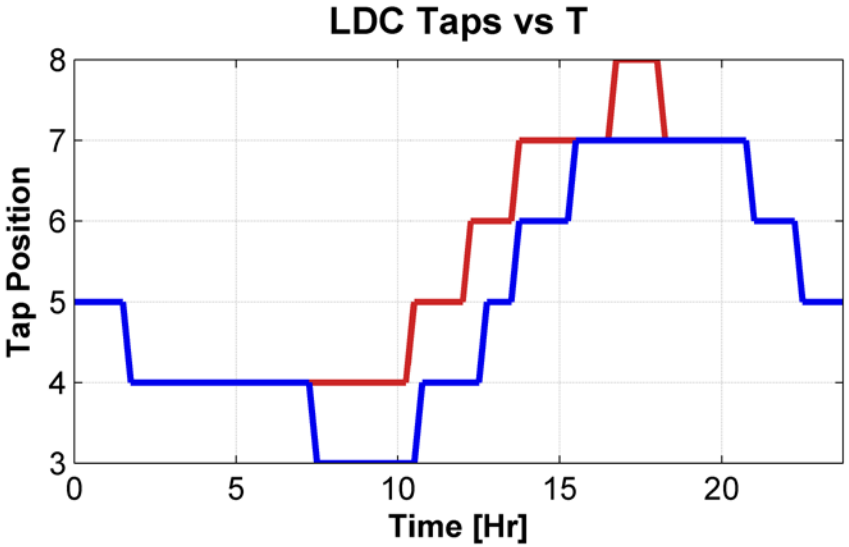
$$I \propto V_{TAP}$$

$$I + I_{PV,est} = (I_{LD} - I_{PV}) + I_{PV,est}$$

We can compensate the current from generation with the LDC measurement to prevent unwanted tap downs.







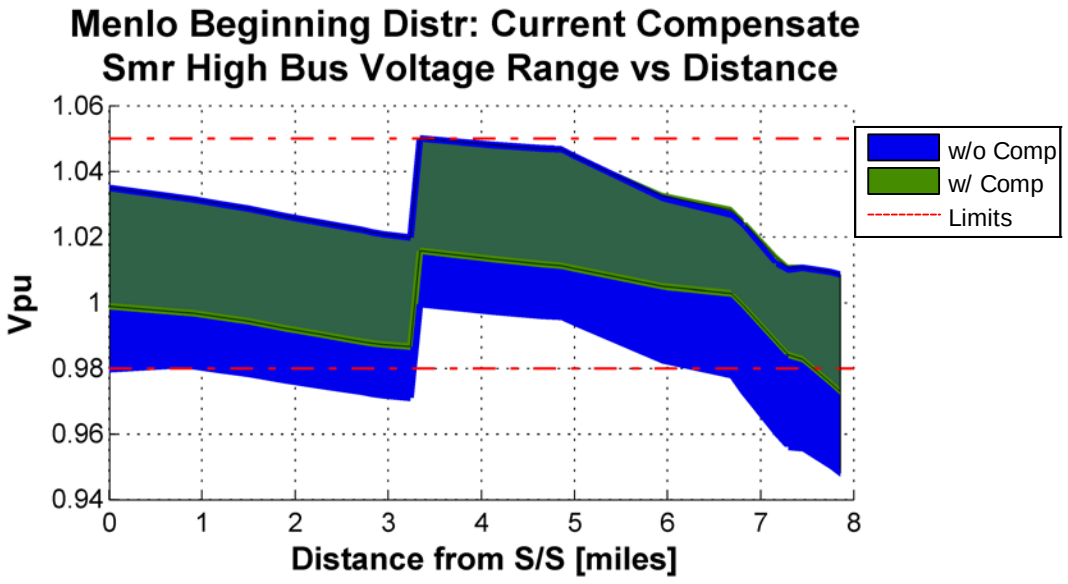
Task 5: Low Voltage - LDC Current Compensation

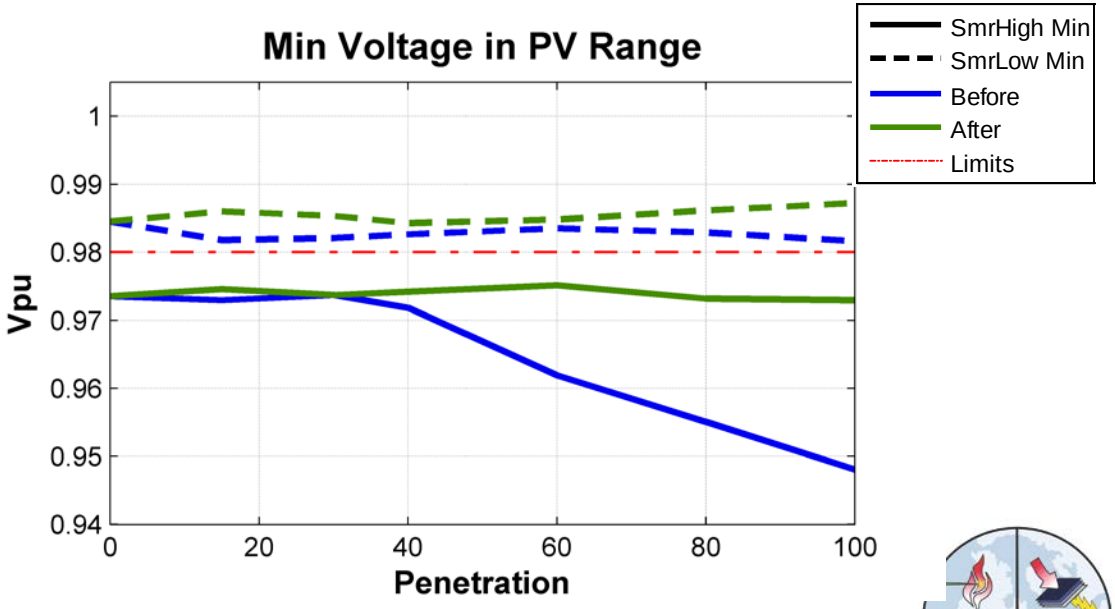
Current compensation simply prevents tap downs due to generation.

Corrects Low Voltage issue for all penetrations

Application:

- Load behind Generation ($\frac{LC}{GC} \geq 1$)
- Estimate PV power generation via:
  - Direct Measurement
  - Insolation measurement
  - Forecast





Task 5 PF Sensitivity

As PV penetration increases, PF decreases in PV region.

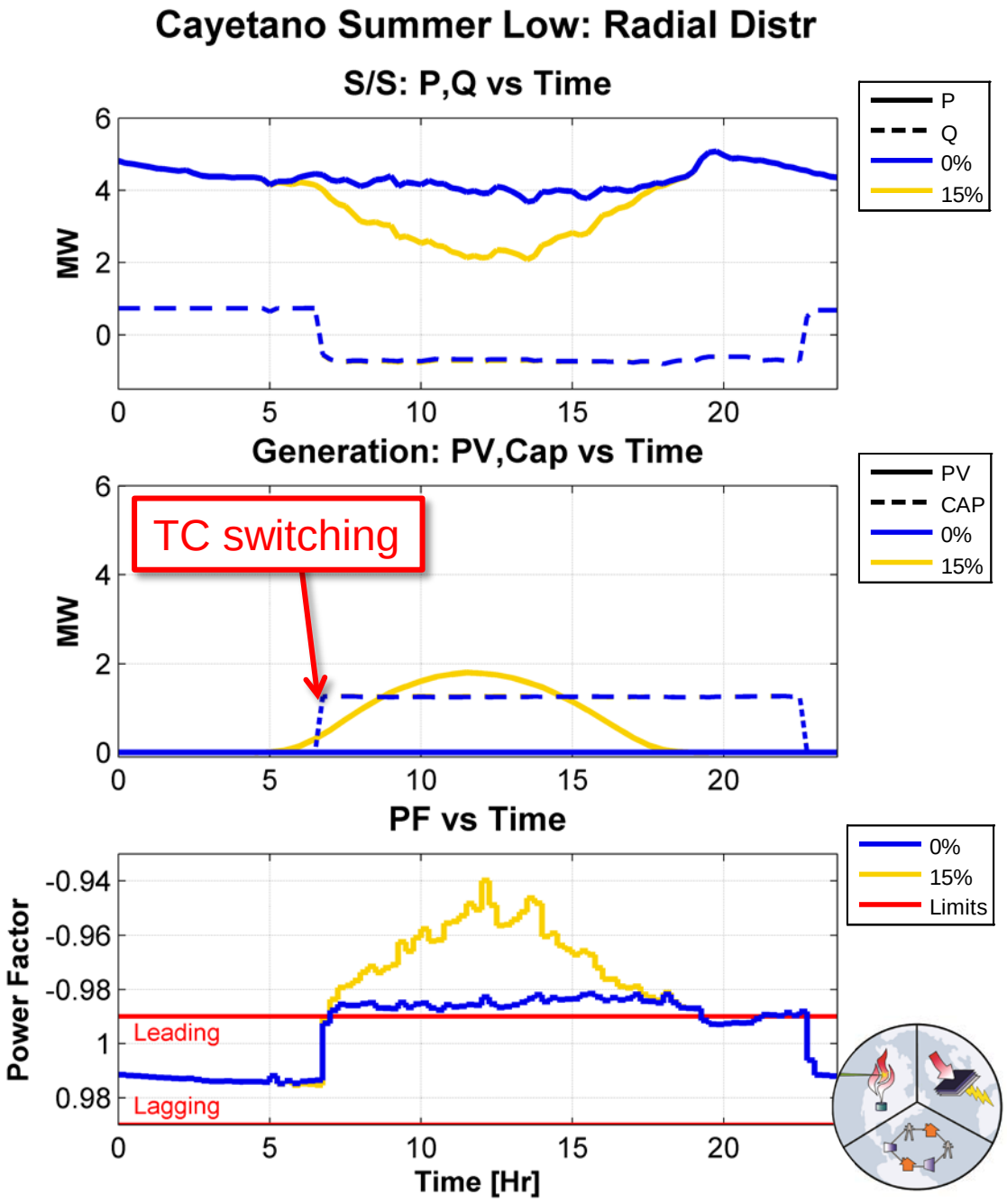
- High Penetrations of PV
- Low Demand

Aggravated by unnecessary capacitor switching

- TC controls

Possible Remedy:

- VAR control capacitor switching



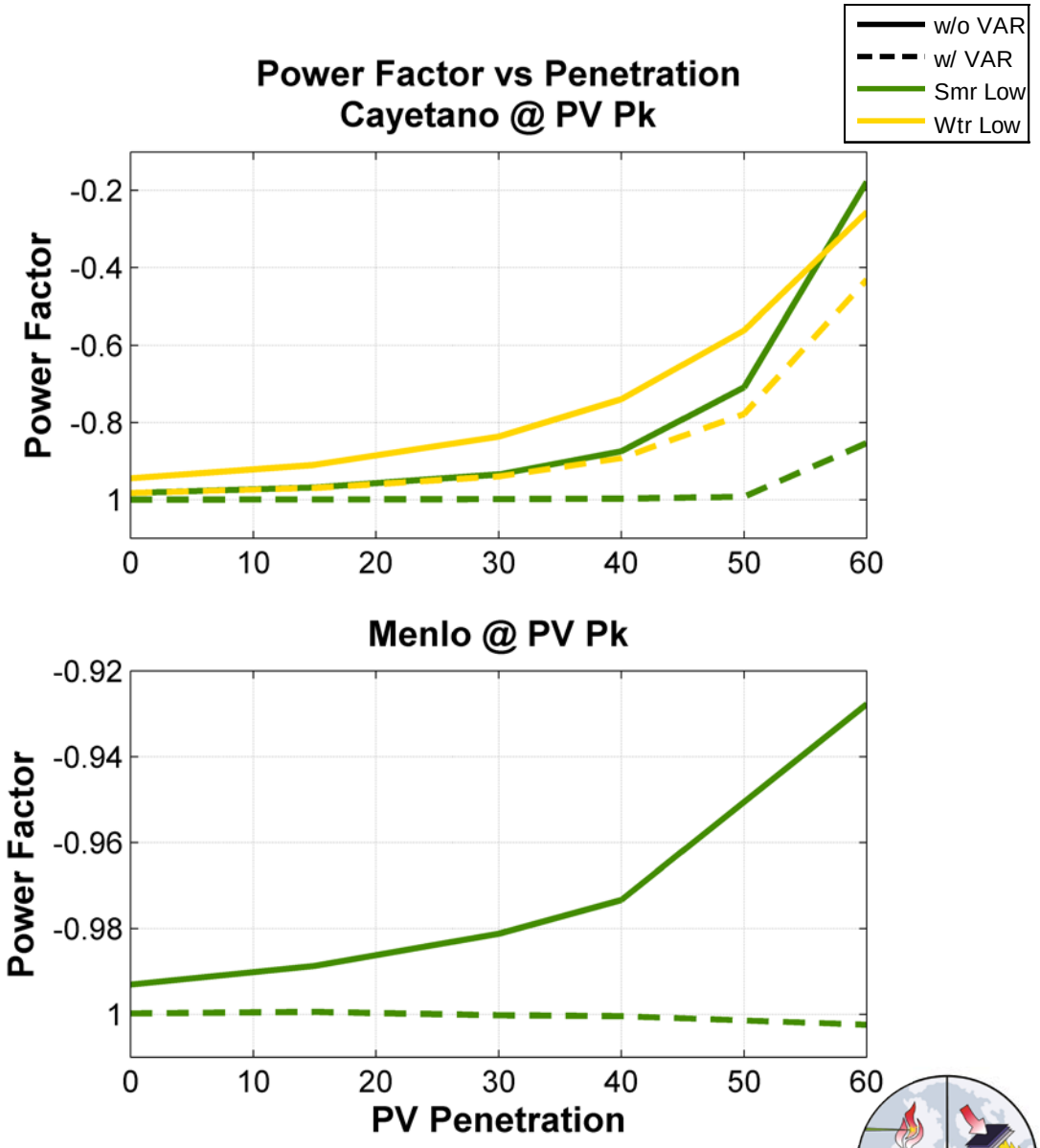
Task 5: PF Sensitivity

VAR capacitor switching controls improvement of PF as penetration increases

PF still sensitive on low load demand days in PV region

Increased switching on high demand days.

Circuit	Char. Day	Total Capacitor Switching	
		Baseline	VAR SW (BL)
Cayetano	Summer High	2	8
	Summer Low	2	0
	Winter High	4	0
	Winter Low	2	0
Menlo	Summer High	9	12
	Summer Low	8	8



Task 5 Summary: Progressive Steps

High Voltage Condition:

- Identification: ❶ High system impedance at bus, ❷ excess generation
- Correction: ① Re-conductor, ① Site Selection

Load Drop Compensation Low Voltage Condition:

- Identification: ❶ Elevated PV penetrations, ❷ Beginning generation distributions, ❸ Middle and End Load Demand distribution
- Correction: ① Lower line impedance (raise system voltage), ② Line Regulator, ③ Discount PV generation from LDC control.

Low Power Factor Condition:

- Identification: ❶ Elevated PV Penetrations, ❷ Low Load Demand
- Correction: ① VAR Controlled Switching Capacitors

Tasks & Key Deliverables

Task 1 Project management

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- Model scenarios and comparisons to grid monitored data

Task 3 Quantify PV integration limits

- Determine limits for PV penetration within existing circuit architectures and with existing technology

Task 4 Advanced inverter control

- Assess the risks and benefits of advanced inverter control

Task 5 Integrated distribution grid control

- Progressively introduce and assess smart integrated distribution technologies/ controls to determine impacts on PV penetration

Task 6 Practical feasibility and outreach

- Determine market potential of technology and encourage adoption

Task 6 Practical Feasibility and Outreach

Overview:

- Met on a monthly basis with PG&E and Itron technical staff to review progress and discuss practical feasibility
- Led a ½ day overview meeting with PG&E and Itron technical staff to critique findings for technical content and practical feasibility
- Prepared for and participated in a technical presentation of findings at the DOE/CPUC High Penetration Solar Forum in San Diego

Task 6 Practical Feasibility and Outreach

Task 3: Quantify PV integration limits

- Determine limits for PV penetration within existing circuit architectures and with existing technology

Evaluation

- Voltage Control Equipment
  - Increased Penetration causes more tap switching
  - No noticeable Capacitor operation change
- High Voltage
  - Excess generation, high line impedance, and the Generated Center located behind Load Center are characteristics of High Voltage.
- Low Voltage
  - The interaction of PV generation and the LDC cause tap downs.
  - (LDC Operation) Generated Center located in front Load Center
- Power Factor Sensitivity
  - As Penetration increases, Sub-Station power factor decreases
- Line Loss
  - Penetration point minimizing line-loss exists

Task 6 Practical Feasibility and Outreach

Task 5: Integrated distribution grid control

- Progressively introduce and assess smart integrated distribution technologies/ controls to determine impacts on PV penetration

Advanced Steps

- Volt/VAR Control
  - Utilize spare capacity to provide reactive power support (D-STATCOM)
  - Increase line capacity
  - May reduce utility voltage control ability
  - May inject local voltage spikes and reduce local line stability

- Active Power Filter (APF)
  - Remove harmonic distortion
  - Adds additional costs to customer

- Technology Progression
  - Incorporation of local area voltage control
  - Inverter communications link
  - Incentives for reactive power compensation

Task 6 Practical Feasibility and Outreach

Task 5: Integrated distribution grid control

- Progressively introduce and assess smart integrated distribution technologies/ controls to determine impacts on PV penetration

Progressive Steps

- High Voltage Condition
  - Through the use the circuit load/generation distribution and construction, High Voltage conditions can be avoided
- Low Voltage Condition
  - Lowering effective line impedance by raising system voltage mitigated Low Voltage condition, but dependent on application.
  - Line Regulator and LDC Compensation can mitigate Low Voltage condition depending on proper application
- Power Factor Sensitivity
  - VAR switching capacitors improve Sub-Station power factor, but the factor will still decrease as PV penetration increases
- Identification of possible issues is essential to enable High Penetrations of PV

CSI RD&D Project Webinar

Thank You!

CSI RD&D Project Webinar

Josh Payne

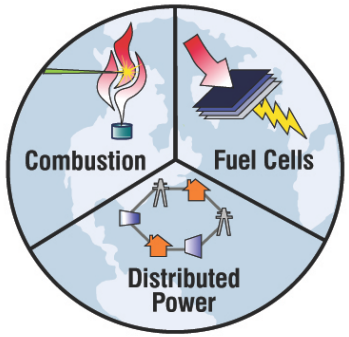
Fei Gu

Professor Jack Brouwer

Professor Scott Samuelsen

Advanced Power and Energy Program

University of California, Irvine, CA



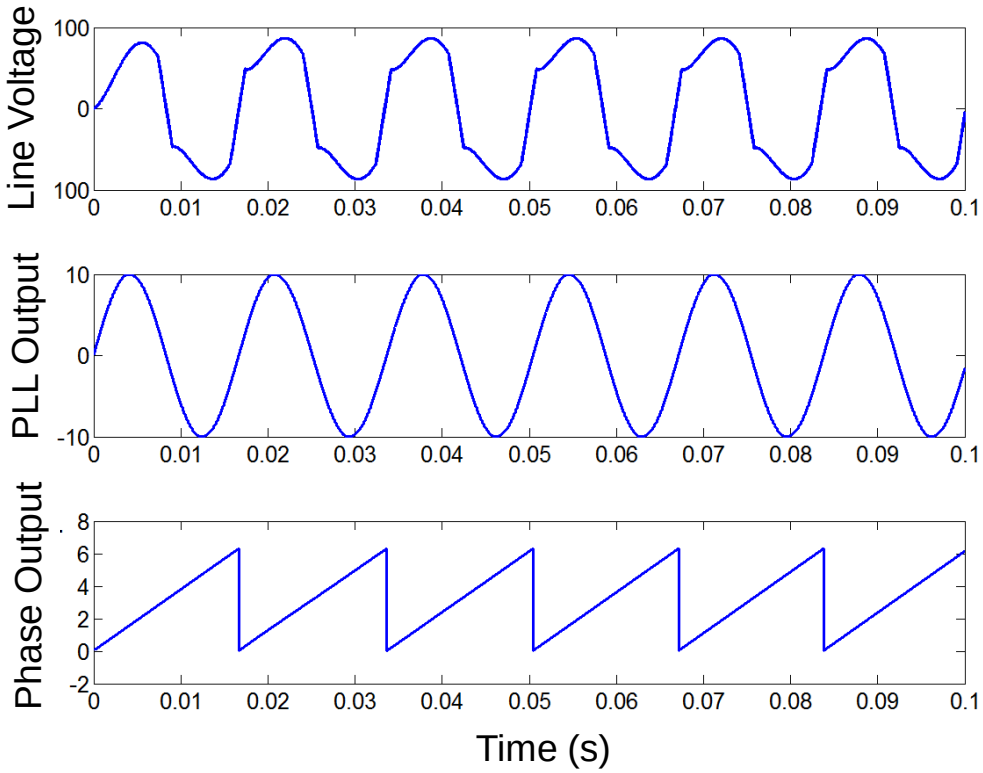
In Collaboration with PG&E

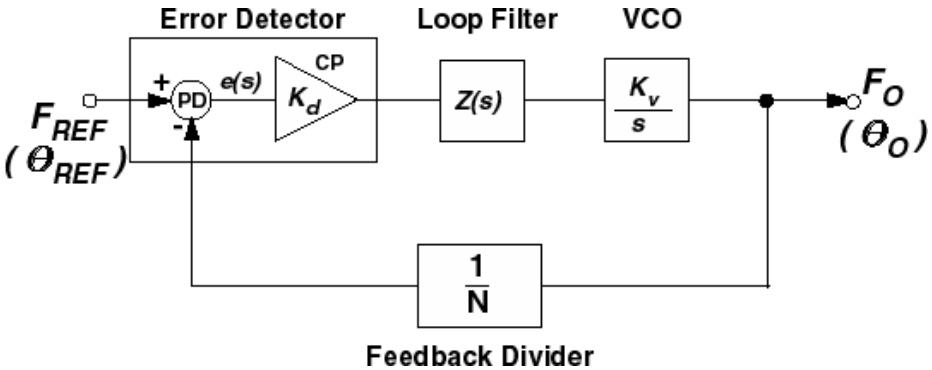
May 14, 2013

Task 4 Model Development

PLL

- **Provides grid synchronization signal**
  - Extracts grid frequency
  - Extracts grid phase
  - Reproduces clean reference signal

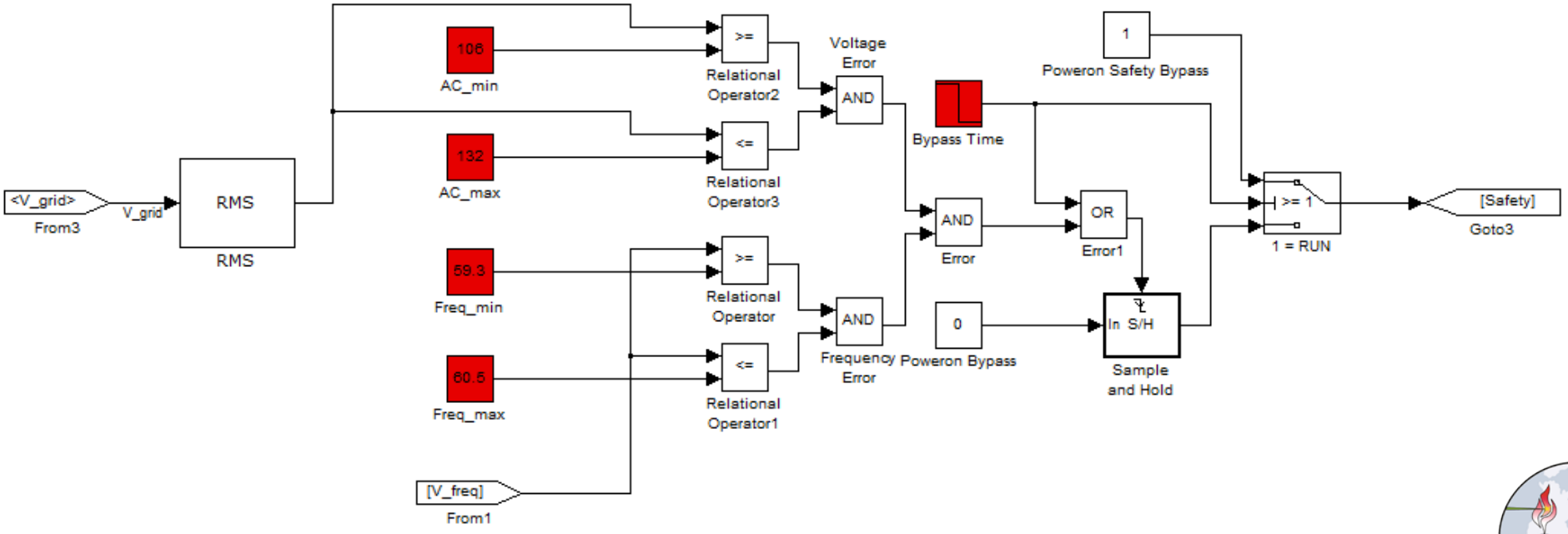




Task 4 Model Development

Anti-Islanding

- **IEEE- Std. 1547 / UL 1741**
  - "Cease to Energize Functionality"
  - Sudden change in system frequency (df/dt)
  - Sudden change in voltage magnitude (dv/dt)
  - Sudden change in power output (dP,dQ/dt)
  - Positive frequency feedback (Sandia shift)
  - **Over-under limits (frequency / voltage)**



Task 4 Model Development

Power Electronics

Output Filter

- **Power Electronics**
  - Full-bridge topology
  - Alternatives
    - H5
    - Bipolar Single Bridge
    - Non-isolated
- **Output Filter**
  - LC Filter
  - Alternatives
    - LCL Filter

Task 4 Model Development

Controller

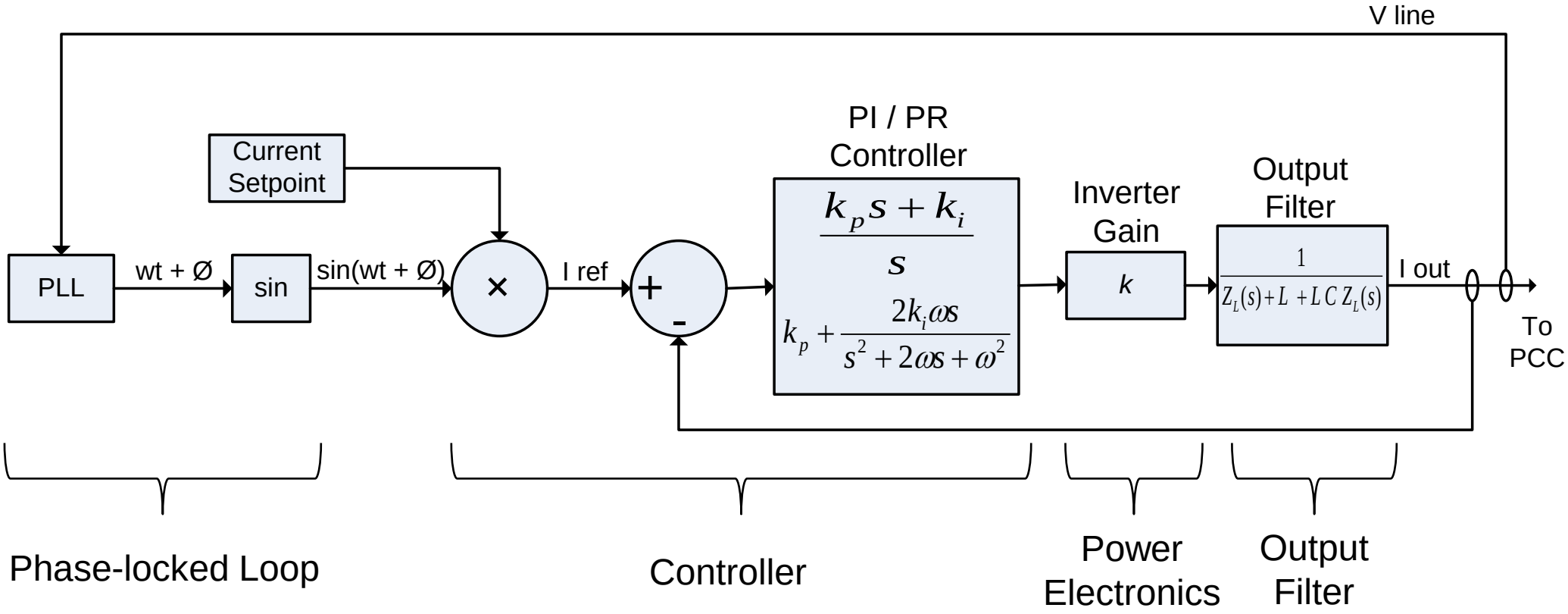
- **Proportional/Integral + Feed-forward (PI)**
  - Simple, robust, well-understood
  - Steady-state tracking error

- **Proportional/Resonant (PR)**
  - Improved steady state tracking error
  - Improved transient performance
  - PR + LCL filters provides lower output ripple
  - Complicated
  - Poor performance when not at exactly 60 Hz

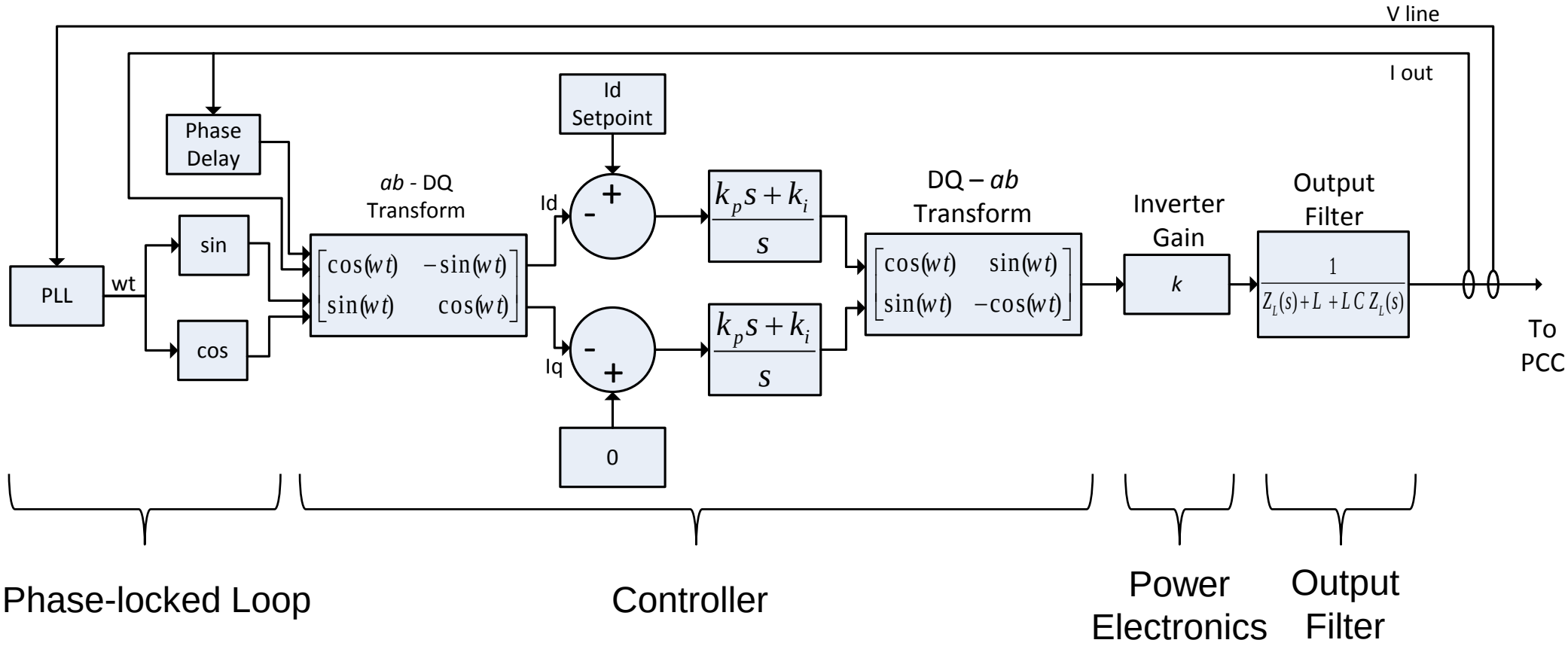
- **Alpha/beta - DQ Transform (DQ)**
  - Widely used in three phase systems
  - Perfect steady state tracking
  - Poor transient performance in single phase systems

Advantage Disadvantage

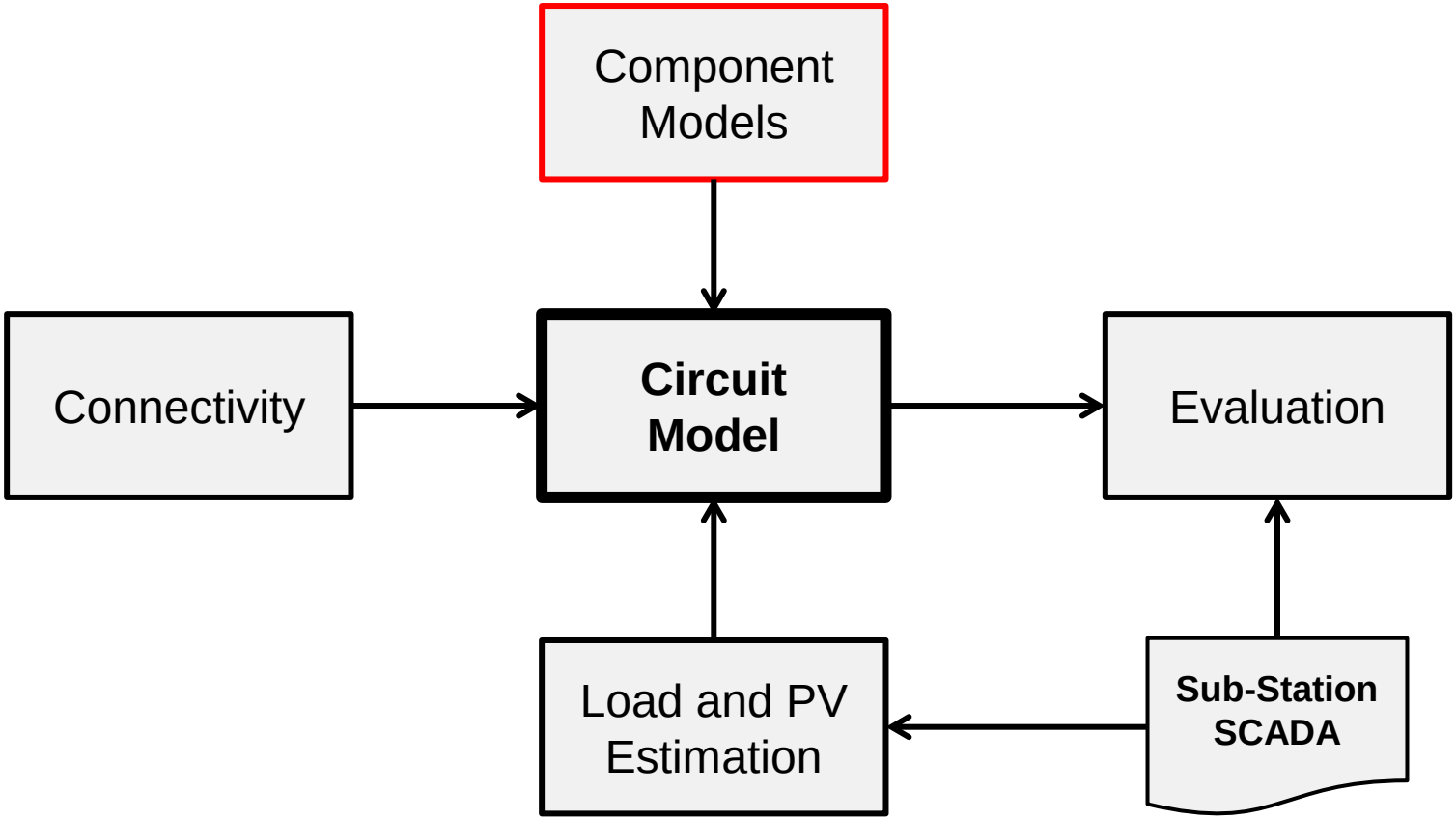
Task 4 Model Development



Task 4 Model Development



Task 2: Model Methods



Task 2: Model Methods – Component Models

Basic

- Bus: $\boldsymbol{V} = \boldsymbol{V}_{US} - \Delta\boldsymbol{V}$

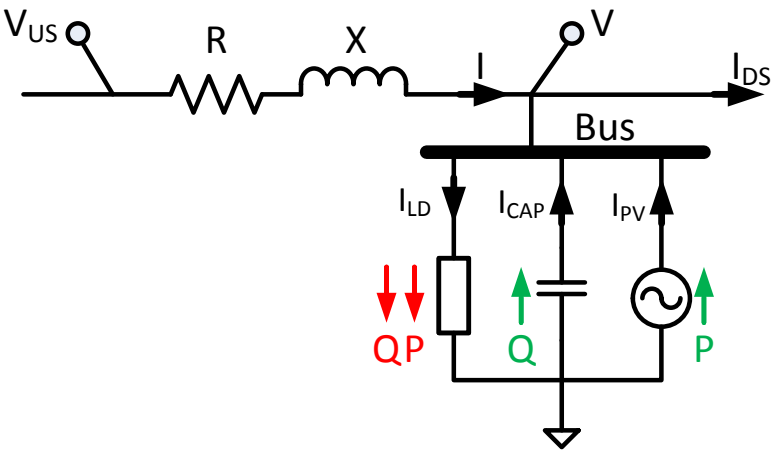
  $\boldsymbol{I} = \boldsymbol{I}_{DS} + \boldsymbol{I}_{LD} - \boldsymbol{I}_{CAP} - \boldsymbol{I}_{PV}$

- Line drop: $\Delta\boldsymbol{V} = \boldsymbol{I} \cdot (R + jX)$

- Load: $\boldsymbol{I}_{LD} = \left(\frac{P+jQ}{\boldsymbol{V}}\right)^*$

- PV: $\boldsymbol{I}_{PV} = \left(\frac{-P}{\boldsymbol{V}}\right)^*$

- Capacitor: $\boldsymbol{I}_{CAP} = \left(\frac{-jQ}{\boldsymbol{V}}\right)^*$



Capacitor switching Controls

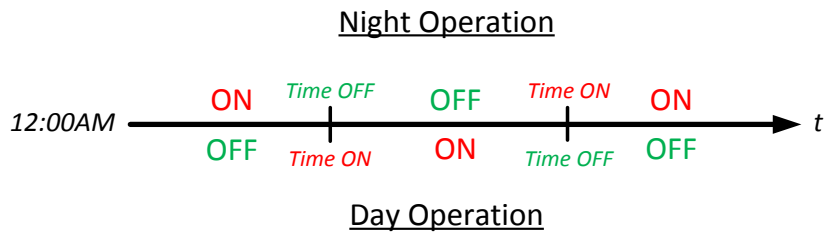
OLTC with LDC

Task 2: Model Methods – Component Models

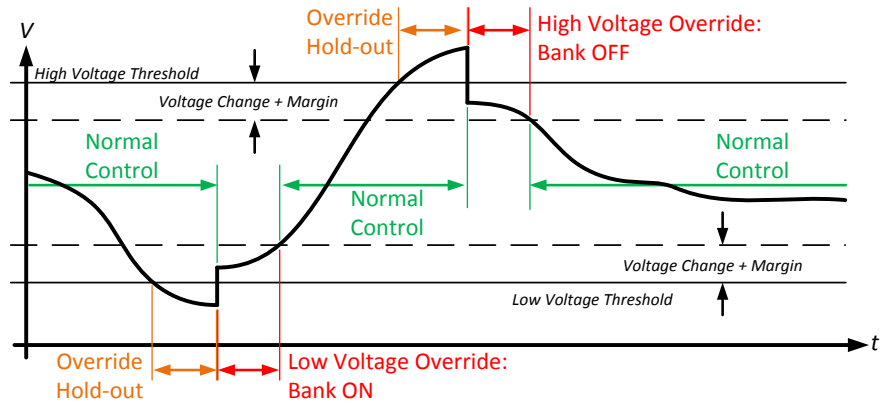
Basic

Capacitor switching Control

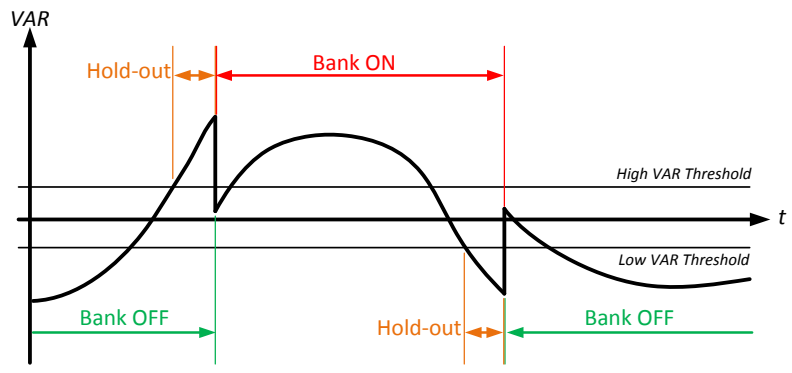
- Time Clock (TC) Control
- Temperature Control
  - Estimated with TC



- Voltage Override (VO) Control
  - Is paired with Time, Temperature or VAR



- VAR Control



Voltage Regulator

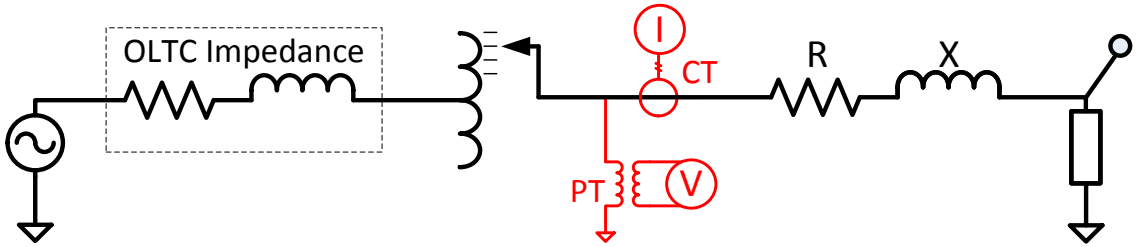
Task 2: Model Methods – Component Models

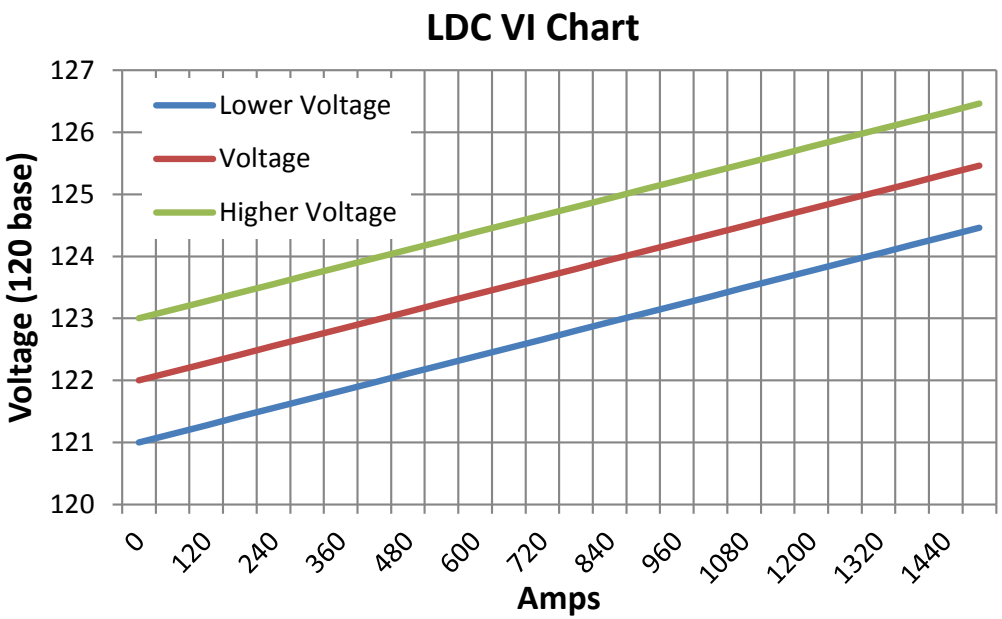
Basic

Capacitor switching Control

Voltage Regulator

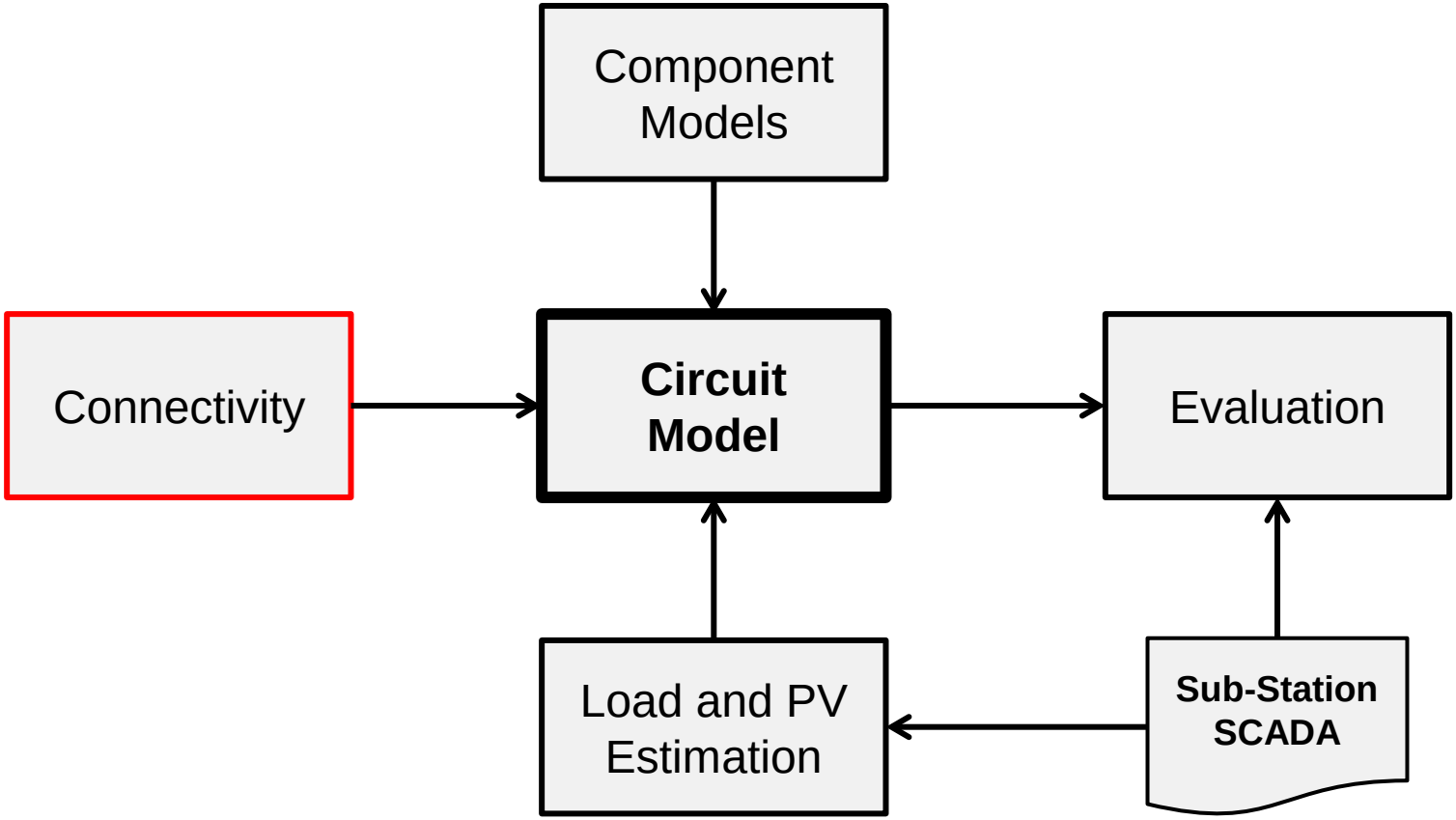
- On-Load Tap Changing Transformer with Load Drop Compensation (OLTC w/ LDC)
- Line Regulator



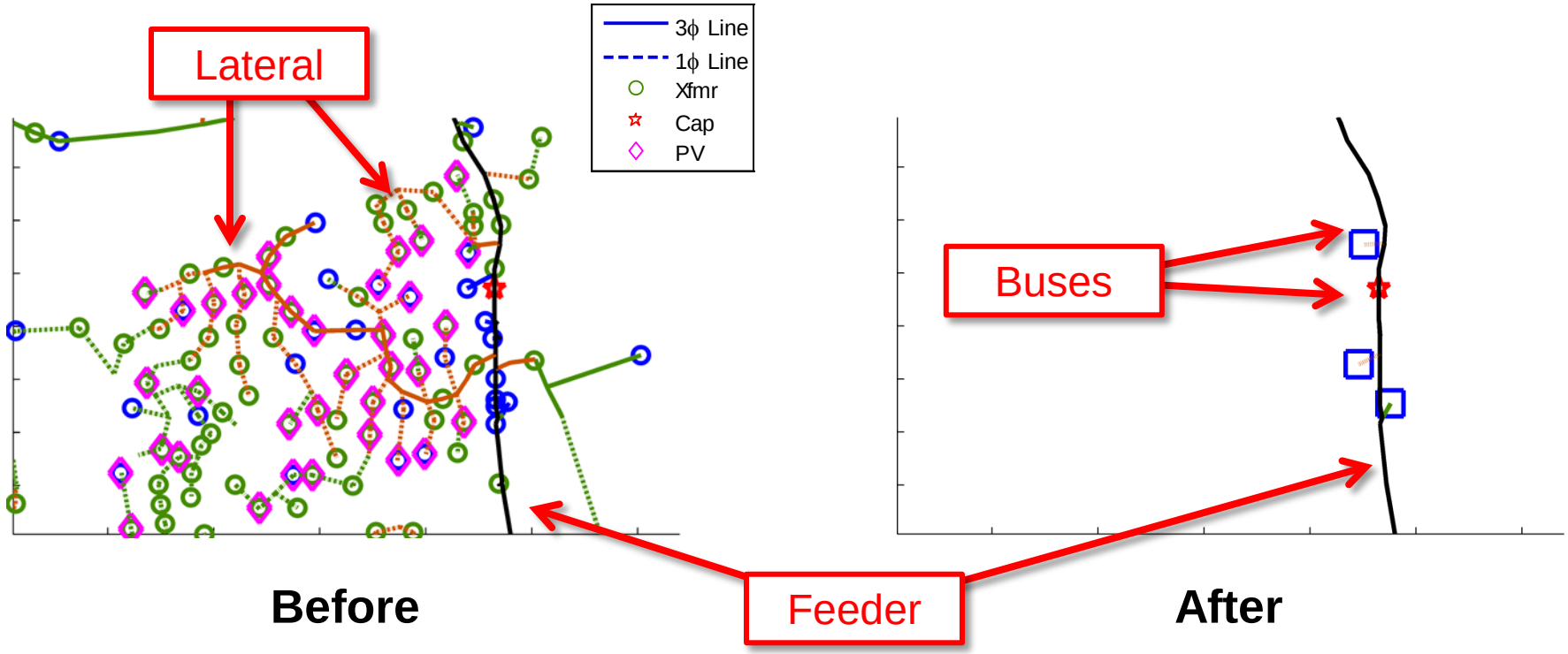


Parameter	Value
Regulation	+/- 10%
Steps	32
VLC	122V
R	3
X	0
Band	+/- 1V
CT	1300
PT	100

Task 2: Model Methods



Task 2: Model Methods – Connectivity



Laterals are aggregated to Feeder to approximate balanced loads

Buses are formed around voltage control equipment to maintain original position

- Capacitors, Boosters, Step-downs

Task 2: Model Methods – Connectivity

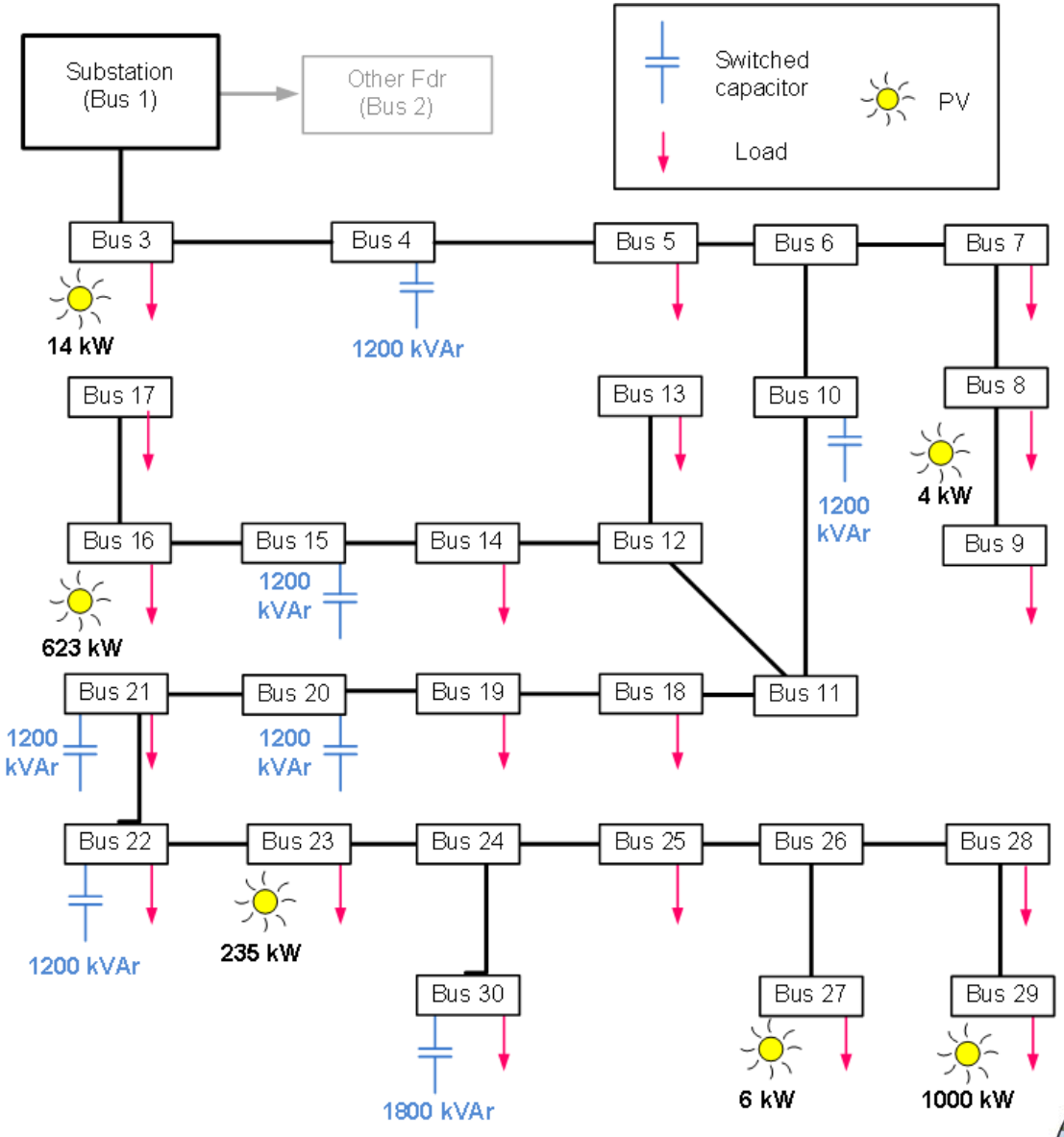
Cayetano 2111

30 bus reduced model

OLTC w/ LDC

7 Switched Capacitors

- Summer:
  - TC (x1)
  - TC w/ VO (x2)
  - Temp (x3)
  - Temp w/ VO (x1)
- Winter:
  - TC (x1)
  - TM w/ VO (x2)
  - Temp (x1)
  - OFF (x3)



Task 2: Model Methods – Connectivity

Menlo 1102

42 bus reduced model

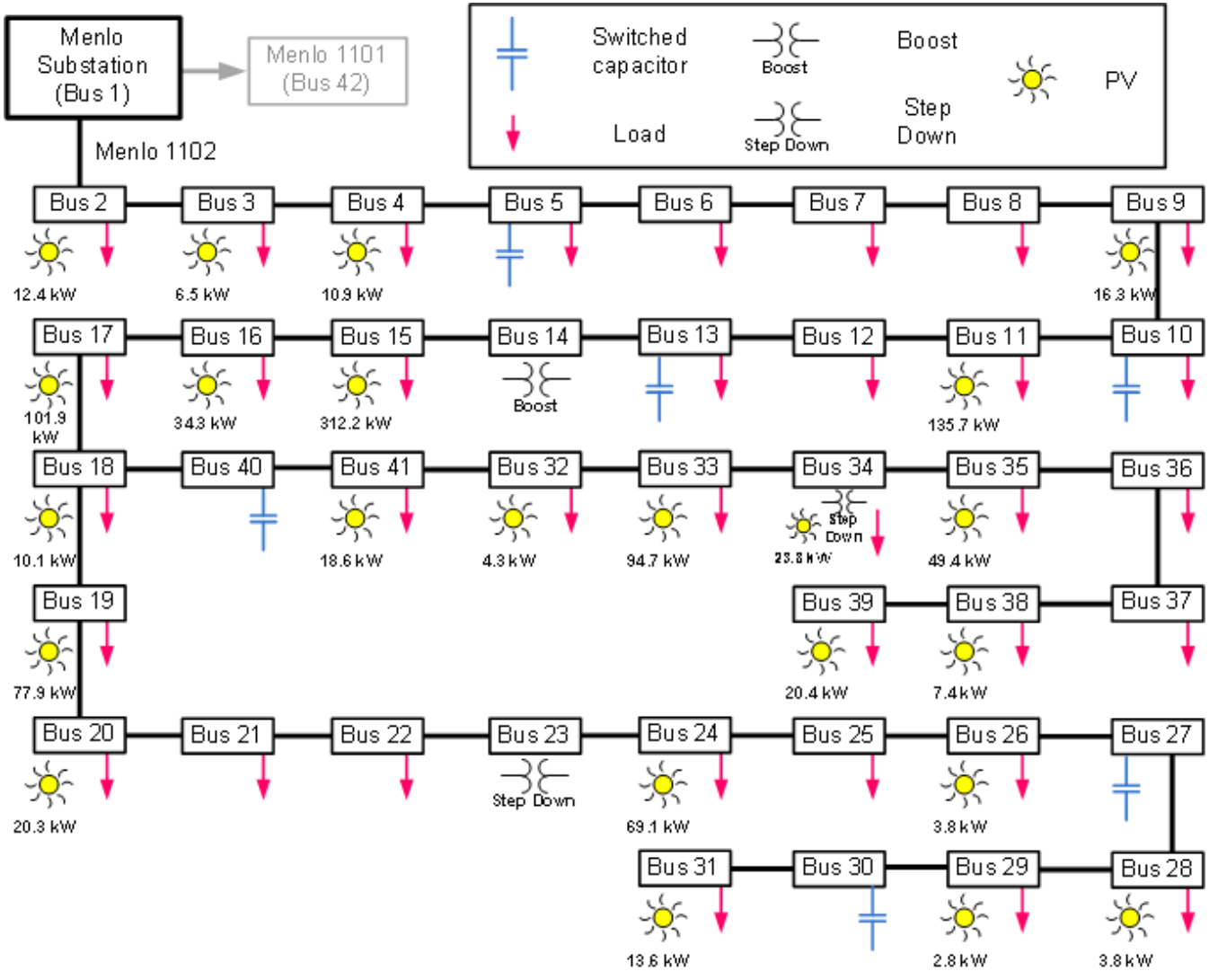
OLTC w/ LDC

6 Switched Capacitors

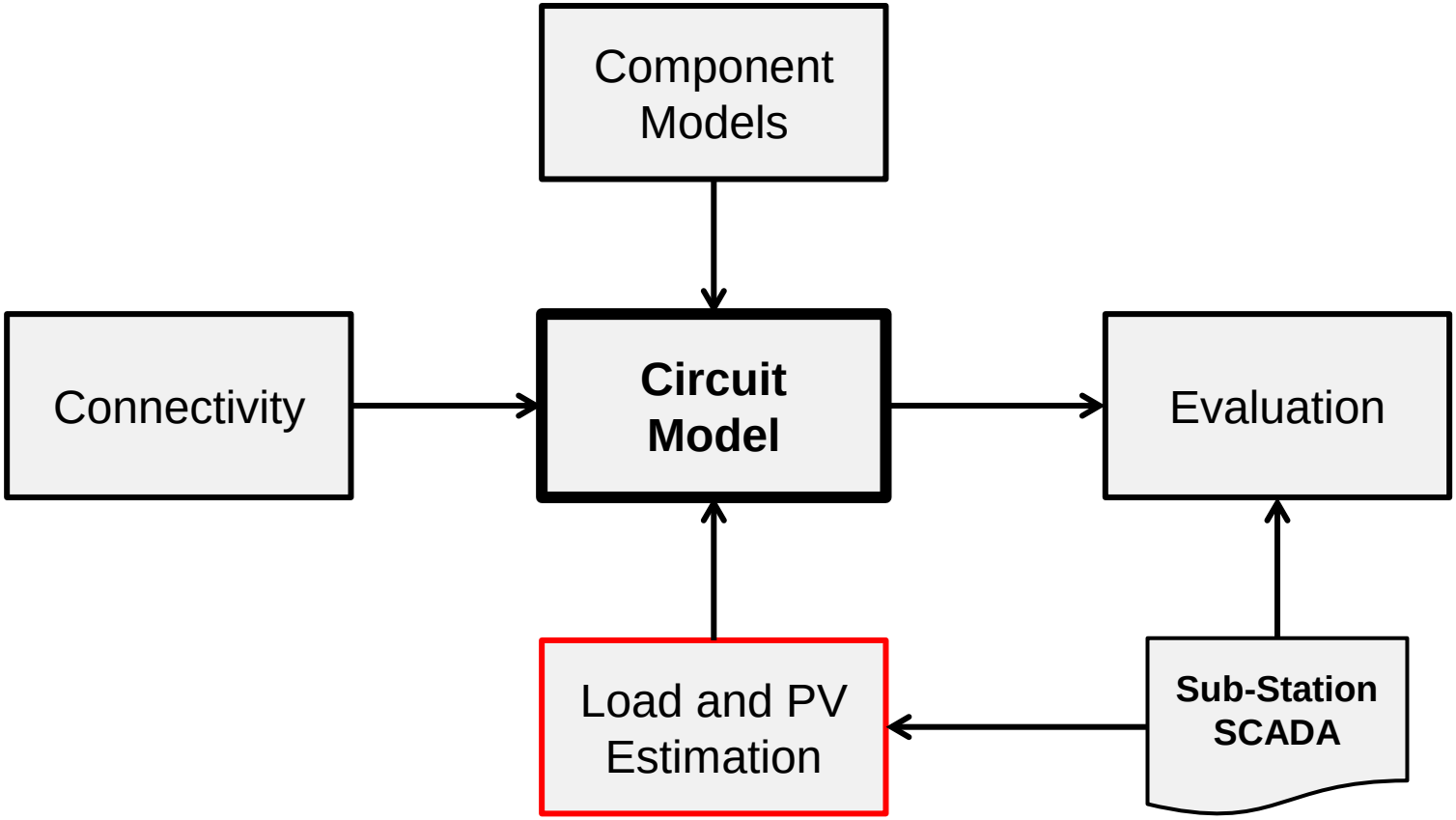
- Summer:
  - TC w/ VO (x4)
  - ON (x1)
  - OFF (x1)
- Winter:
  - TC w/ VO (x3)
  - Temp w/ VO (x1)
  - ON (x2)

3% Booster

2 Step-Downs



Task 2: Model Methods



Task 2: Model Methods – PV/LD Estimation

Sub-Station (S/S) Real and Reactive Power is used as input into the circuit models

- The Load Demand must first be decoupled by estimated PV generation (more later)
- Characteristic Days are selected to evaluate control equipment on extreme days

The circuit model iteratively derives the bus voltage and current based on the load demand inputs

- S/S Current and Voltage used to evaluate the accuracy of the model

Feeder	Real Power (P)	Reactive Power (Q)	Line-to-Neutral Voltage			Line Current		
			A	B	C	A	B	C
Cayetano 2111	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Menlo 1102	Yes	Yes	No	No	No	Yes	Yes	Yes

Task 2: Model Methods – PV/LD Estimation

Consistency of SCADA evaluated using the following formula:

$$S = \sqrt{P^2 + Q^2} = V_{ln} \cdot I_{a+b+c}\ [VA]$$

Cayetano results:

- Valid Days: 344 (94%)
- Invalid Days: 20 (6%)

Menlo results

- Valid Days: 138 (38%)
- Invalid Days: 227 (62%)

Only the summer season was evaluated for the Menlo circuit

Task 2: Model Methods – PV/LD Estimates

Measured data from Substation SCADA system

- Real Power (P_{SCADA})
- Reactive Power (Q_{SCADA})
- Voltage (V)
- Current (C)

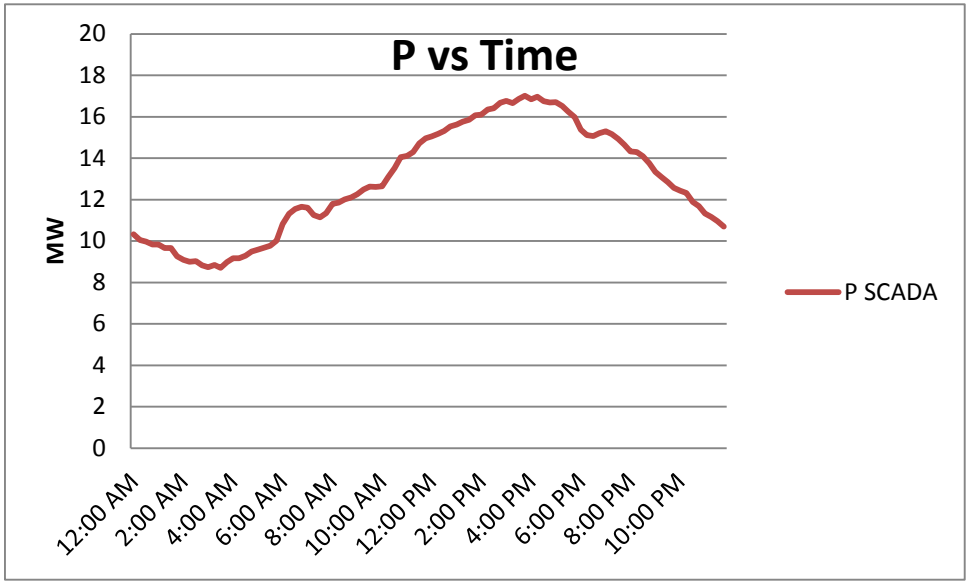
Generation in circuit estimated

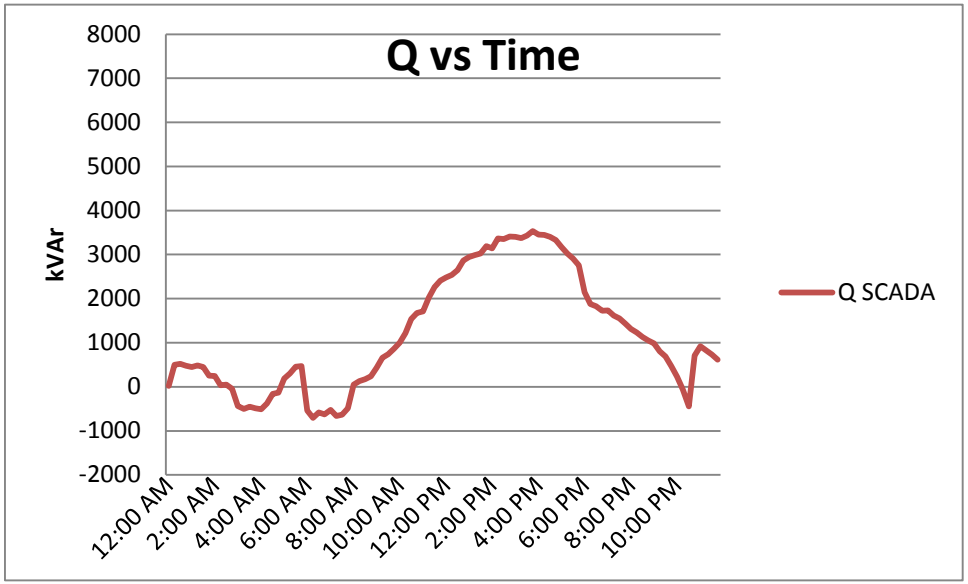
Initial Load Demand is derived

$$P_{SCADA} + P_{PV} \approx P_{LD}$$

$$Q_{SCADA} + Q_{CAP} \approx Q_{LD}$$

Measured





Information provided by PG&E

Task 2: Model Methods – PV/LD Estimates

Measured data from Substation SCADA system

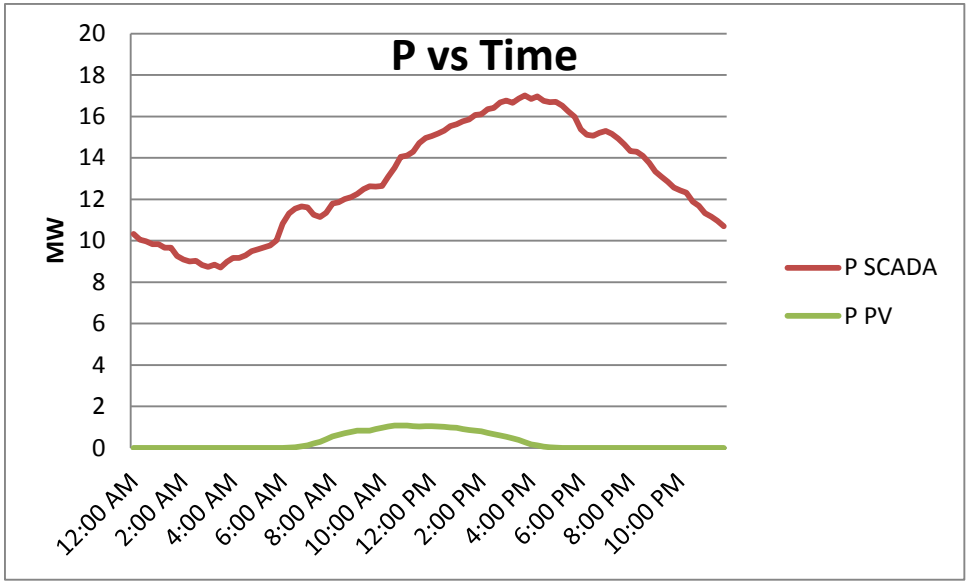
Generation in circuit estimated

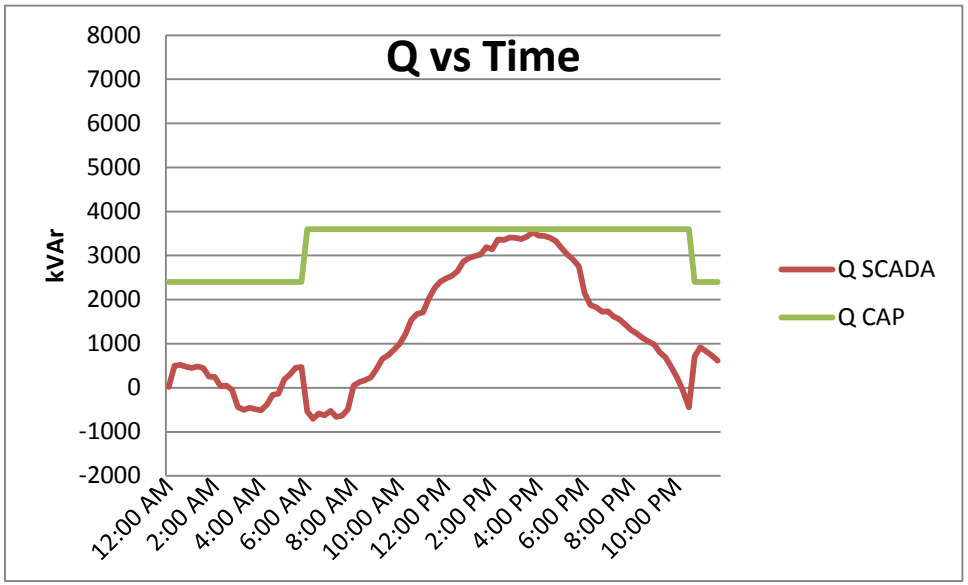
- PV from SolarAnywhere insolation data
- Cap Switching from circuit information

Initial Load Demand is derived

$$\underbrace{P_{SCADA}}_{\text{Measured}} + \underbrace{P_{PV}}_{\text{Estimated}} \approx P_{LD}$$

$$\underbrace{Q_{SCADA}}_{\text{Measured}} + \underbrace{Q_{CAP}}_{\text{Estimated}} \approx Q_{LD}$$





Information provided by PG&E

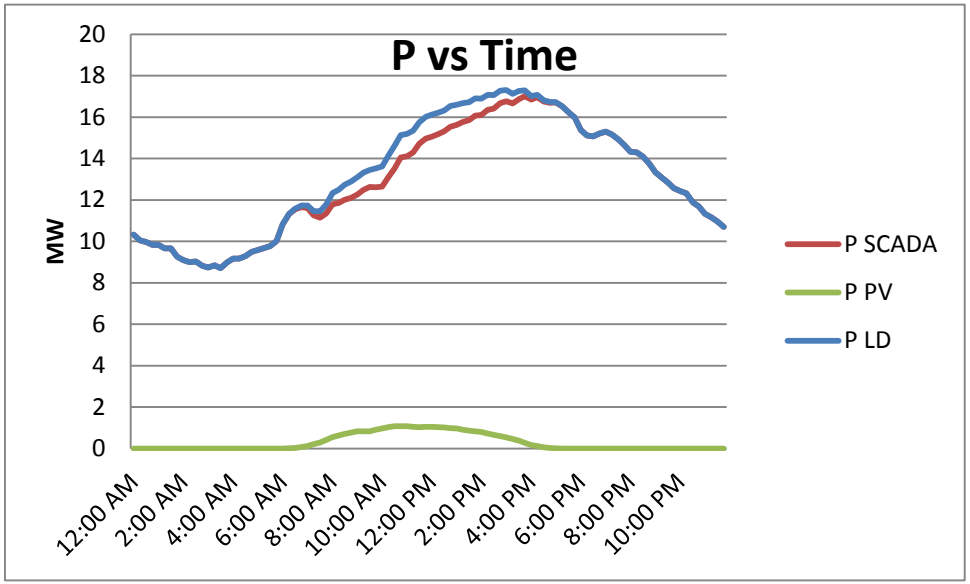
Task 2: Model Methods – PV/LD Estimates

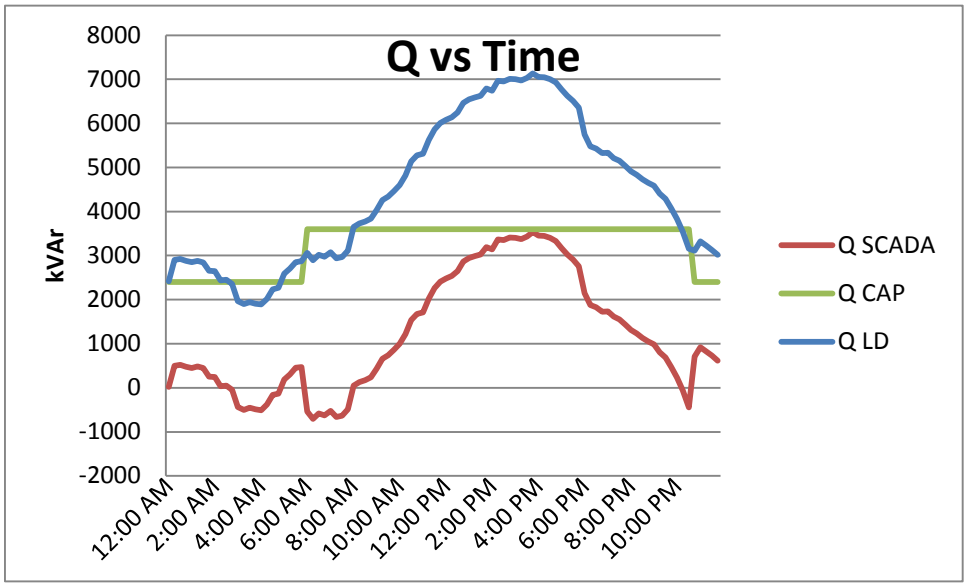
Measured data from Substation SCADA system

Generation in circuit estimated

Initial Load Demand is derived

- Calibration accounts for power consumed by line-loss





$$\underbrace{P_{SCADA}}_{\text{Measured}} + \underbrace{P_{PV}}_{\text{Estimated}} \approx \underbrace{P_{LD}}_{\text{Derived}}$$

$$\underbrace{Q_{SCADA}}_{\text{Measured}} + \underbrace{Q_{CAP}}_{\text{Estimated}} \approx \underbrace{Q_{LD}}_{\text{Derived}}$$

Information provided by PG&E

Task 2: Model Methods – PV/LD Estimates

Characteristic Day Criteria:

High Day

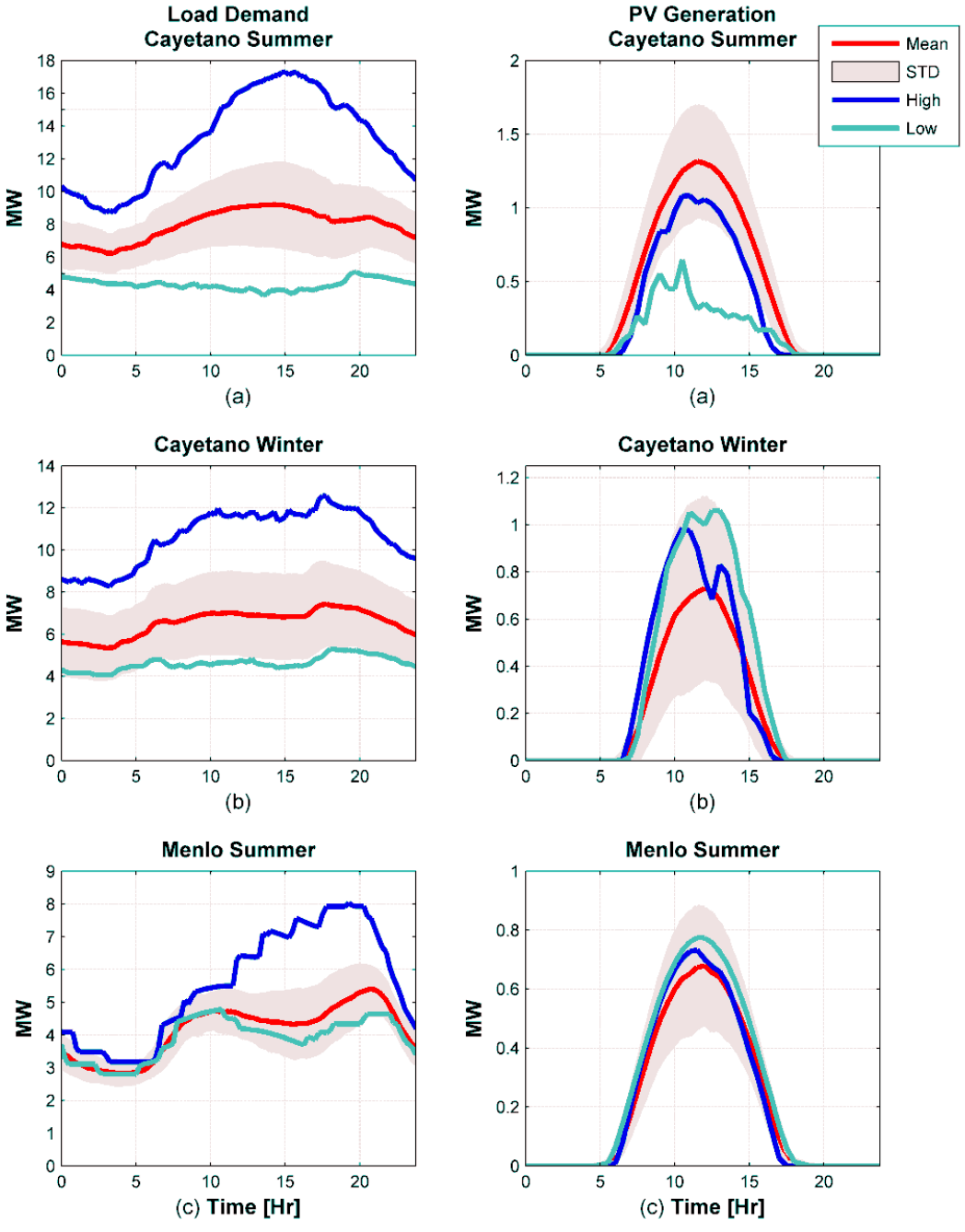
- 1 STD above seasonal average
- PV less than 1 STD of seasonal mean

Low Day

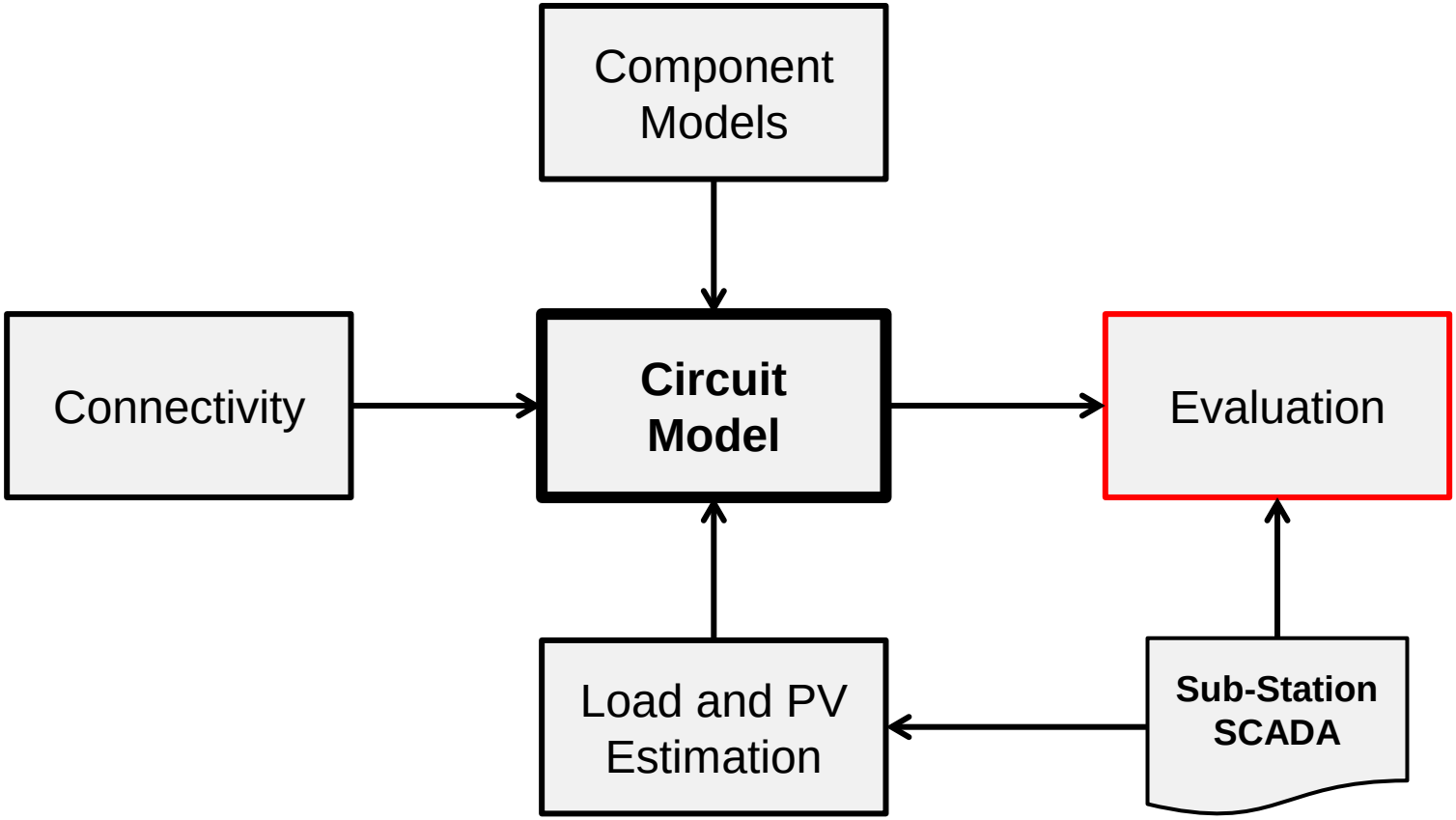
- 1 STD below seasonal average
- PV less than 1 STD of seasonal mean

Selected Days

Cayetano Smr High:	10-14-10
Cayetano Smr Low:	4-4-10
Cayetano Wtr High:	11-8-10
Cayetano Wtr Low:	2-14-10
Menlo Smr High:	9-28-10
Melo Smr Low:	7-2-10



Task 2: Model Methods



Task 2: Model Development – Evaluation

The next step is to calibrate the model to account line losses.

- Performed iteratively until the model output matches the Sub-Station Real and Reactive Power measurements.

To evaluate if the characteristic day model is representative, other prospective character days are selected and used a input to the model.

- The S/S real power, reactive power, voltage, and current simulation error is compared by computing the Normalized Root Mean Square Error (NRMSE) of the signal.

$$NRMSE = \frac{\sqrt{\frac{\sum_{t=1}^{96}\left(x_{SCADA,t} - x_{SIM,t}\right)^2}{96}}}{x_{SCADA,max} - x_{SIM,min}}$$

Task 2: Model Development – Evaluation

The average NRMSE error remained below 15%

- Capacitor switching is the result of higher reactive power error, but the limits are satisfactory

Circuits	Char Day	Compare Days	Average NRMSE (%)			
			P	Q	V	I
Cayetano	Smr High 10-14-10	10/13/10 10/15/10	1.5	6.4	1.3e-6	2e-5
	Smr Low 4-4-10	4/6/10 4/7/10 4/9/10	0.15	15	5.4e-6	3.9e-5
	Wtr High 11-8-10	11/10/10 11/11/10 11/16/10	0.44	12	2.7e-6	2.8e-5
	Wtr Low 2-14-10	2/28/10 1/10/10 3/13/10	4.5e-2	8.2	4.8e-6	3.8e-5
Menlo	Smr High 9-28-10	9/27/10 10/12/10 10/13/10	0.25	8.7	-	5.4e-6
	Smr Low 7-2-10	7/31/10 8/4/10 8/14/10	0.39	10.3	-	39e-6

Task 2: Summary

To evaluate High Pen PV, a 3-phase balanced model was used with predictive voltage control models.

6 Characteristic days models where developed to evaluate High Pen PV utilizing connectivity and Sub-Station measurements.

Commercial Circuit: Cayetano 2111

- Summer High
- Summer Low
- Winter High
- Winter Low

Residential Circuit: Menlo 1102

- Summer High
- Summer Low

Task 3: Concepts – PV

PV Penetration is the ratio of installed PV capacity to yearly load demand peak

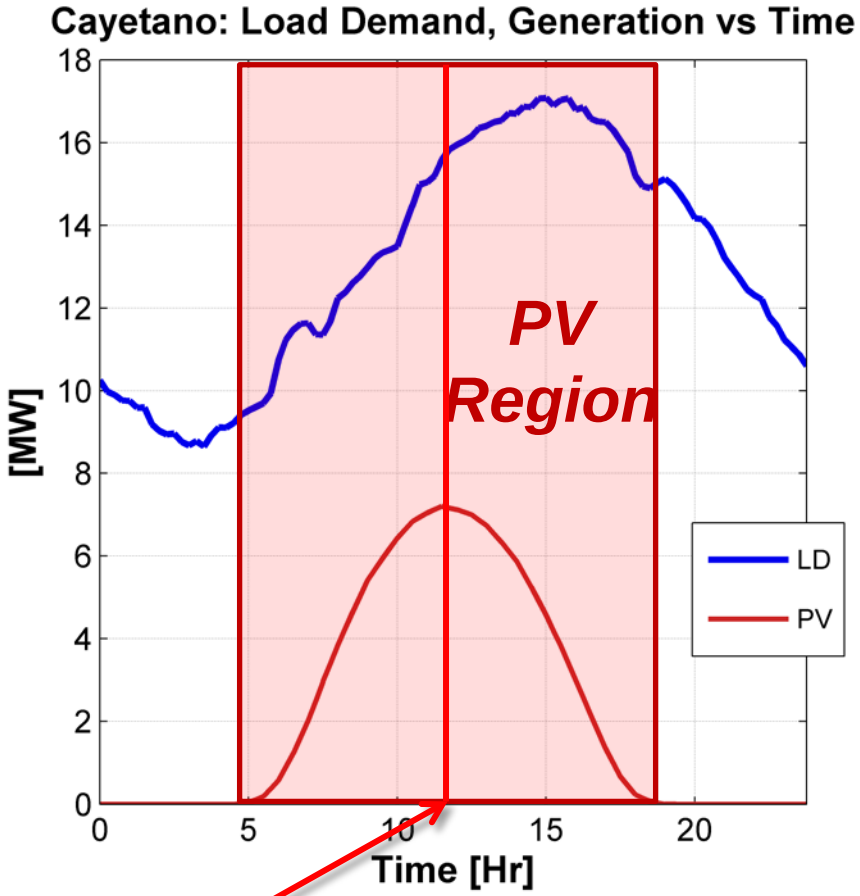
$$Penetration = \frac{PV\ Nameplate}{Peak\ Load\ Demand}$$

PG&E Rule 21 Definition

- Cayetano Peak Load Demand: 12 MW
- Menlo Peak Load Demand: 9.1 MW

The PV Region is the period during the day when PV installations are generating power

- Influence of High Pen PV will occur in this region
- Peak Sensitivity to PV will occur at peak generation



Peak Sensitivity

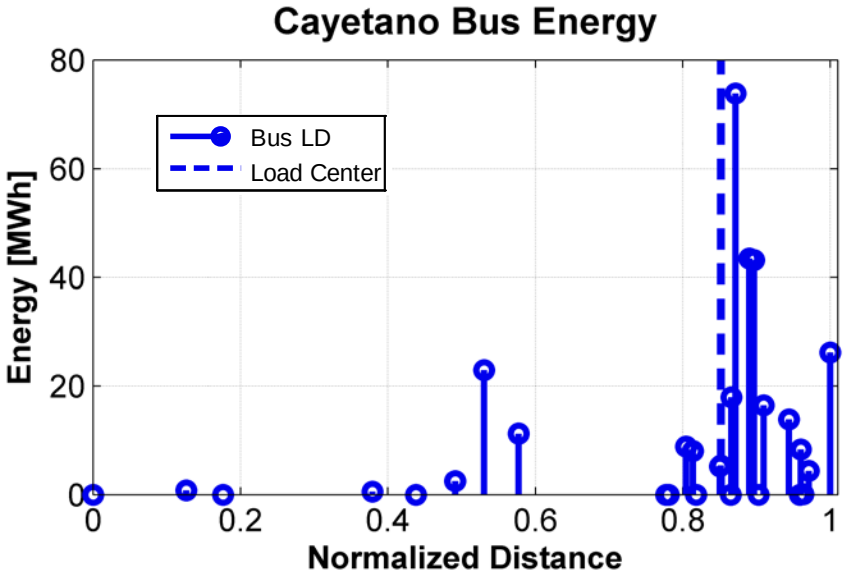
Task 3: Concepts – Load/Generation Distribution

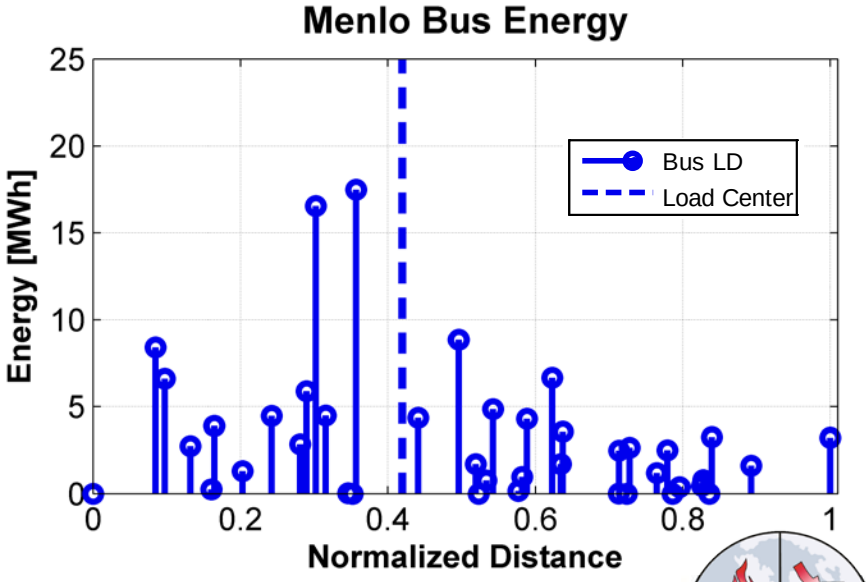
The Load Center (LC) is the average of bus load demand weighted by the normalized distance from the Sub-Station.

$$Load\ Center = \frac{\sum_i E_{LD,i} d_i}{\sum_i E_{LD,i}}$$

- $i = 1,2,\ldots,Total\ Bus\ Count$
- $E_{LD,I} = Total\ Day\ Energy\ consumed\ at\ Bus\ "i"$

Circuit	Load Center
Cayetano	0.85
Menlo	0.42





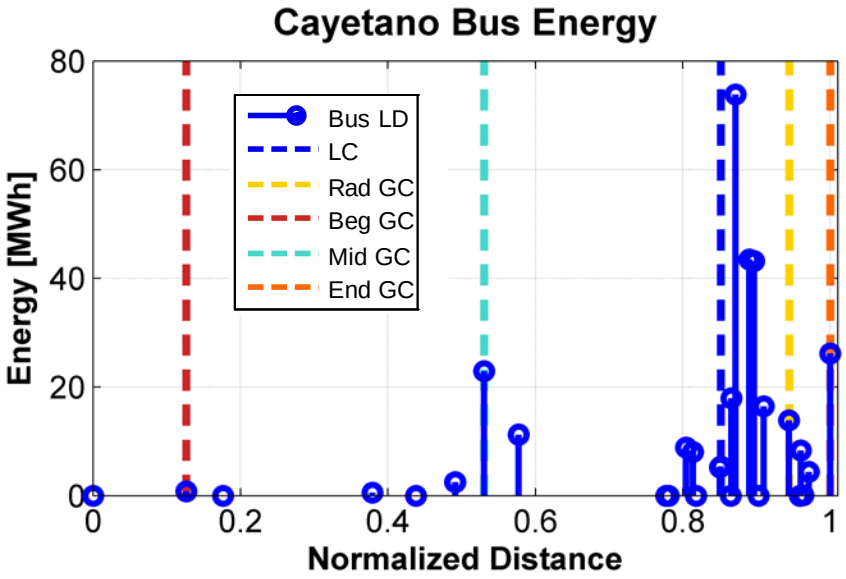
Task 3: Concepts – Load/Generation Distribution

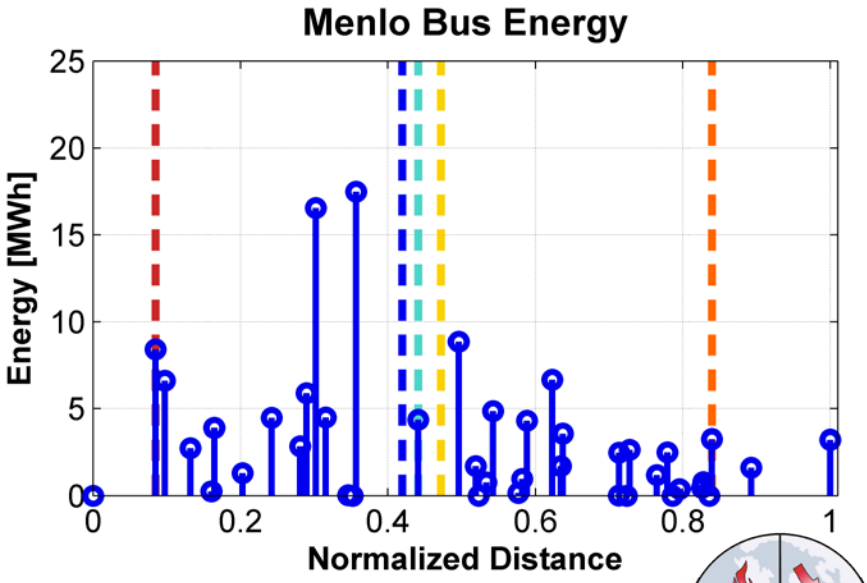
The Generation Center (GC) is the average of bus PV generation weighted by the normalized distance from the Sub-Station.

$$Generation\ Center = \frac{\sum_i E_{PV,i} d_i}{\sum_i E_{PV,i}}$$

- $i = 1,2,\ldots,Total\ Bus\ Count$
- $E_{PV,I} = Total\ Day\ Energy\ generated\ at\ Bus\ "i"$

PV Distribution





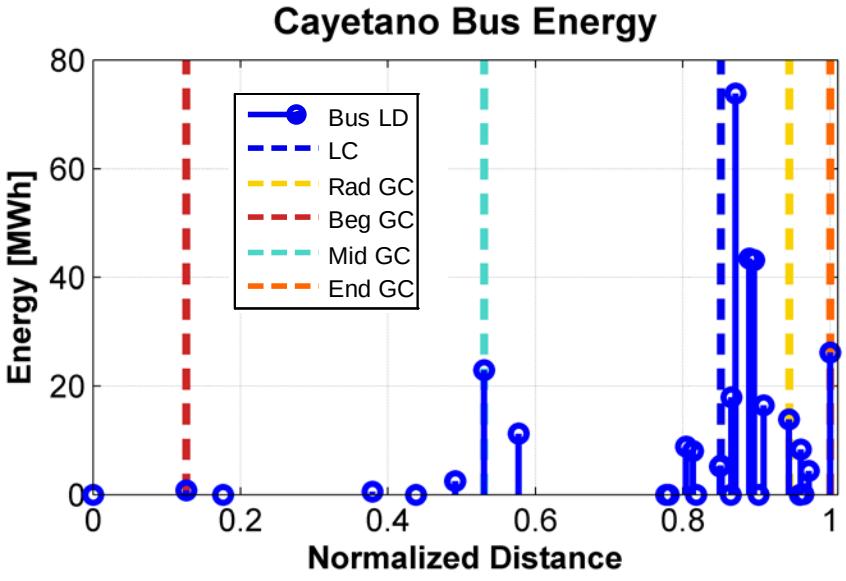
Task 3: Concepts – Load/Generation Distribution

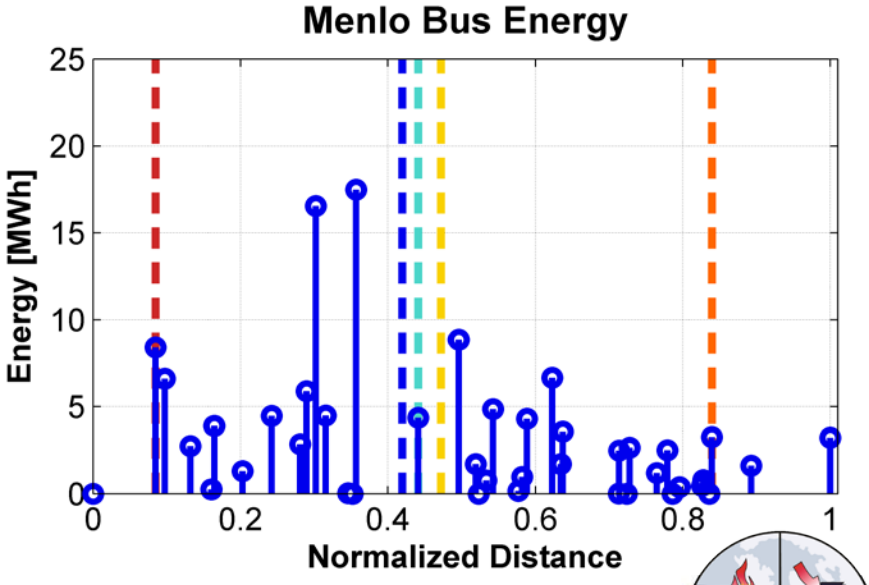
The Generation Center (GC) is the average of bus PV generation weighted by the normalized distance from the Sub-Station.

PV Distribution

- Radial: Proportional increase at existing installation
- Beginning: Lumped at beginning of circuit
- Middle: Lumped at middle of circuit
- End: Lumped at end of circuit

Circuit	Distribution	Generation Center
Cayetano	Radial	0.94
	Beginning	0.13
	Middle	0.53
	End	1
Menlo	Radial	0.47
	Beginning	0.08
	Middle	0.44
	End	0.83





Task 3: Concepts – Reverse Power Flow

PV installations follows grid voltage

- Modeled as a current source

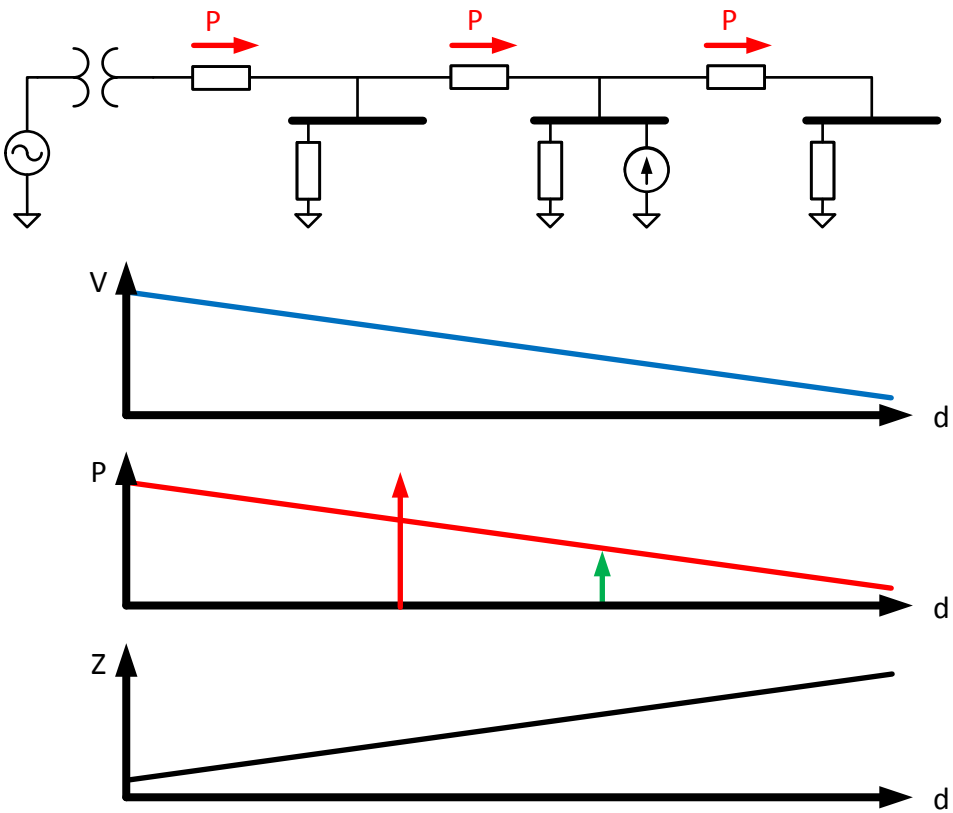
Power Flow dictated by current

$$I = \frac{V_1 - V_2}{Z_{LN}}$$

PV generation will flow*:

1. Locally
2. "Down-stream"
3. "Up-stream"

*Assuming 1) PV is a current source and
2) Circuit is radial.



Task 3: Concepts – Reverse Power Flow

PV installations follows grid voltage

- Modeled as a current source

Power Flow dictated by current

$$I = \frac{V_1 - V_2}{Z_{LN}}$$

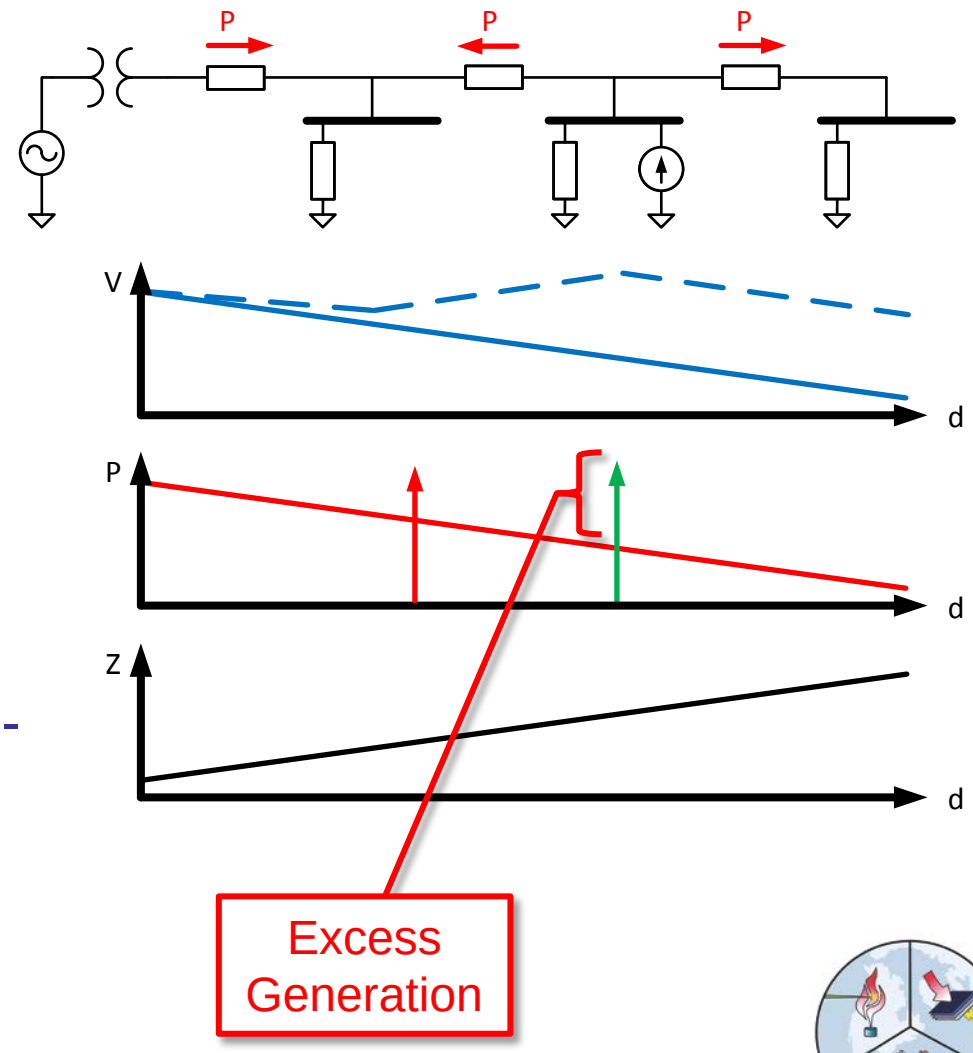
PV generation will flow*:

1. Locally
2. "Down-stream"
3. "Up-stream"

Excess Generation is the surplus generation after the 1) local and 2) "Down-stream" is supplied.

PV installation will *raise* local voltage to enable reverse power flow of excess generation over line impedance

*Assuming 1) PV is a current source and 2) Circuit is radial.



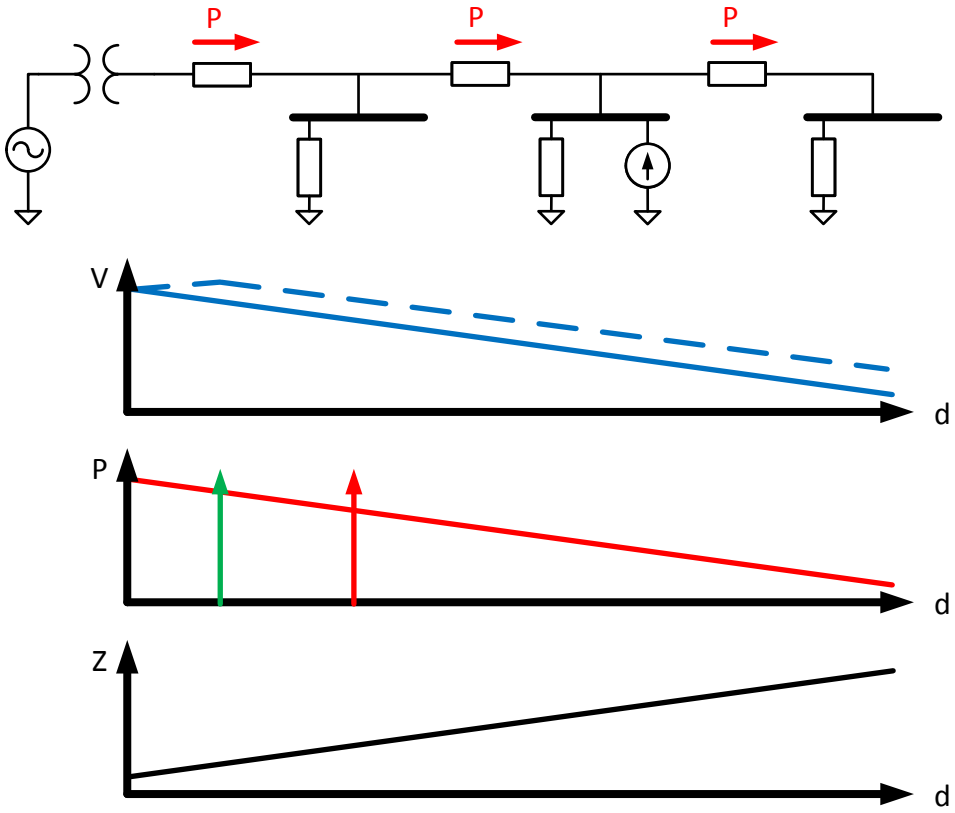
Task 3: Low Voltage

Generation at Beginning of circuit

- Excess generation at higher penetrations
- Low impedance line between GC and S/S

Marginal voltage support

“Fools” LDC controls (more later)



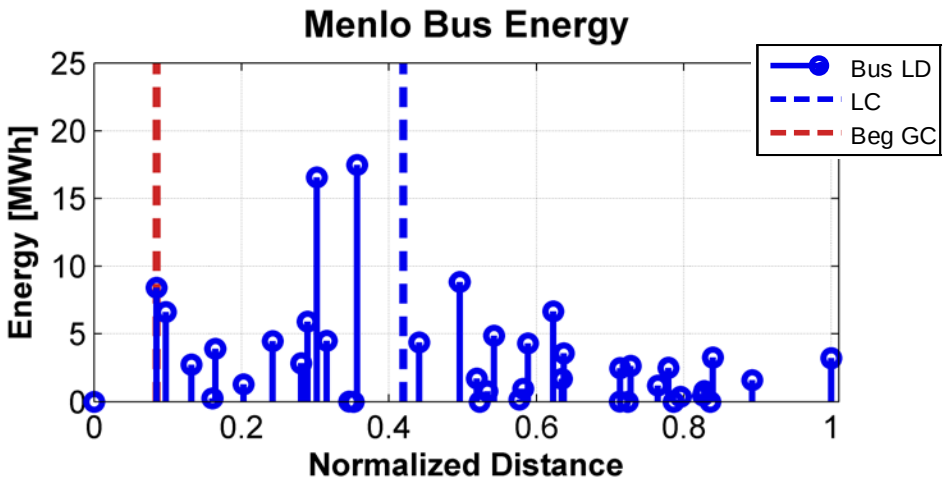
Task 3: Low Voltage

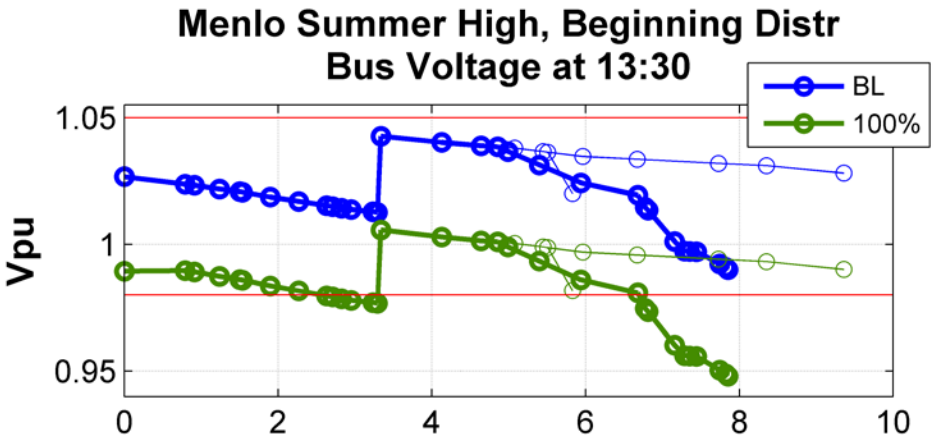
PV providing marginal voltage support

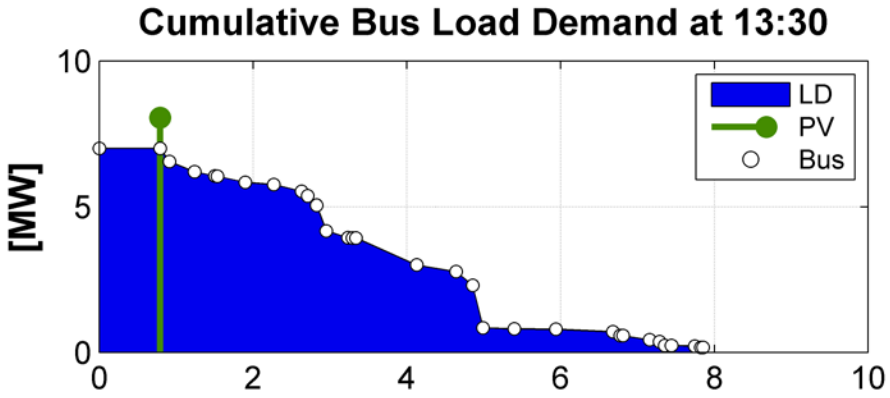
- Entire circuit load demand is located down-stream
- LC is behind GC

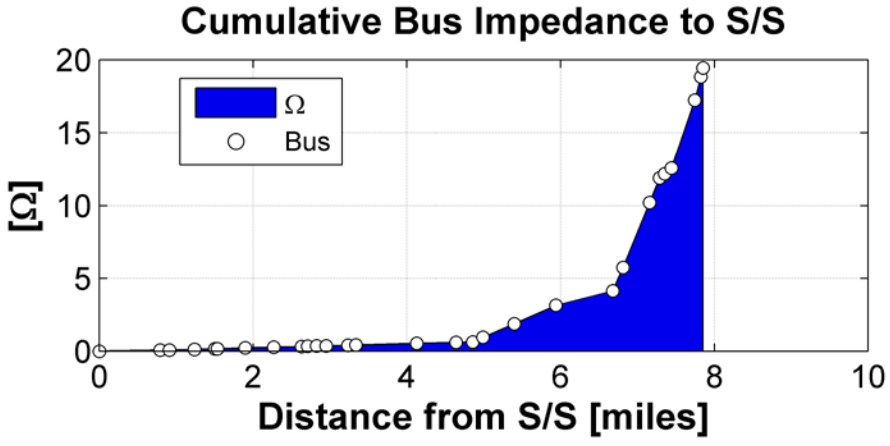
The voltage profile remained the same except translated down.

- Beginning PV distribution is causing LDC to “Tap Down” (more later)









Task 3: Voltage – Summary

Cayetano did not feature voltage issue for all cases

- Due primarily to low impedance line

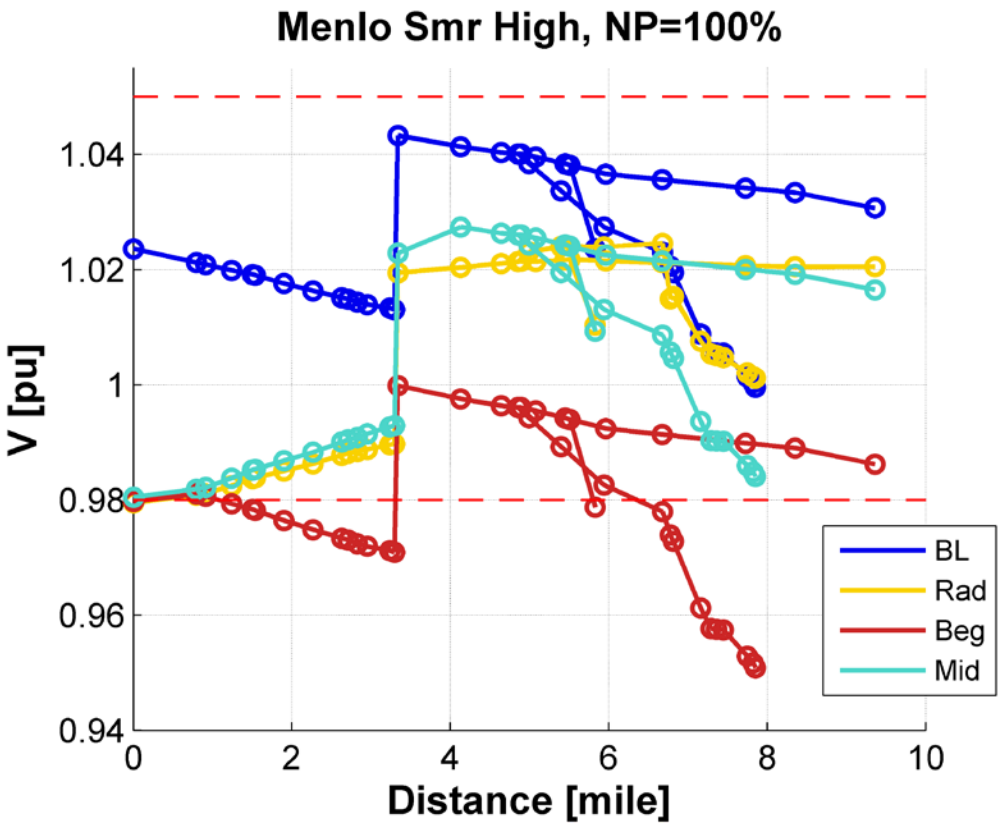
Menlo featured both High Voltage and Low Voltage problems

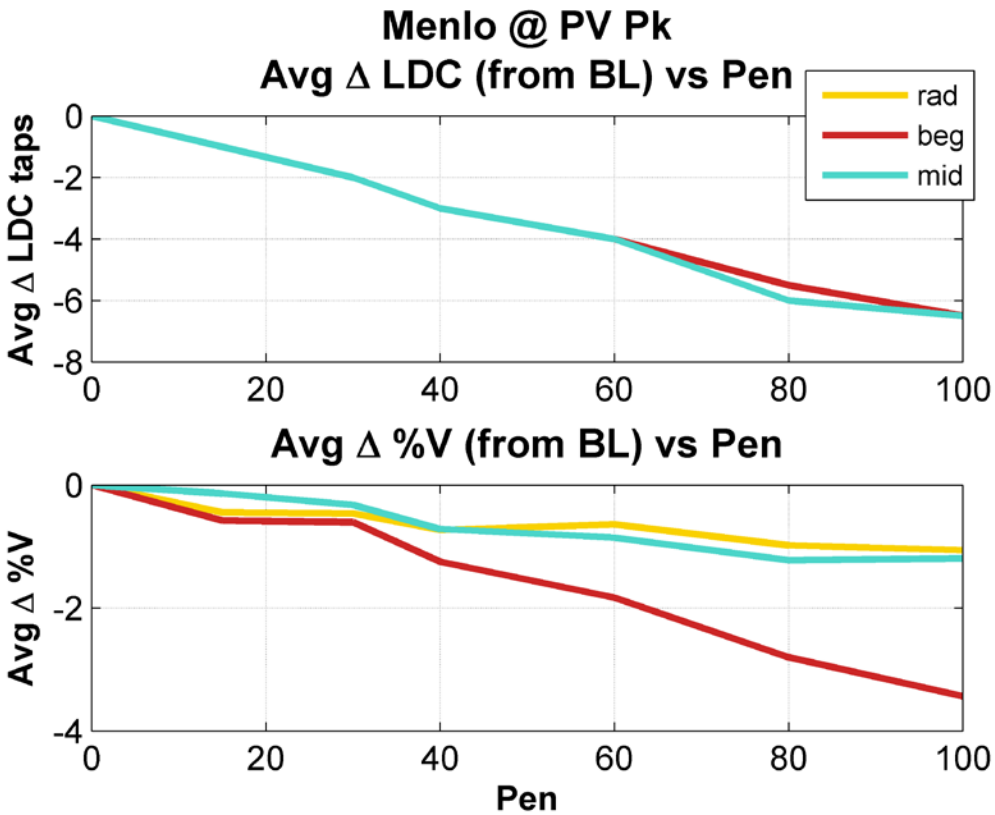
- Problems aggravated by high line impedance

Line Impedance is critical in PV siting

Circuit	Distribution	LC/GC
Cayetano (LC = 0.85)	Radial	0.9
	Beginning	6.54
	Middle	1.6
	End	0.85
Menlo (LC = 0.42)	Radial	0.89
	Beginning	5.25 ← Low Voltage
	Middle	0.95
	End	0.51 ← High Voltage

Task 3: Control Equipment - OLTC w/ LDC





Radial and Middle Distributions:

- $\frac{LC}{GC} < 1$

Beginning Distributions:

- $\frac{LC}{GC} \geq 1$