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Quantification of Risk of Unintended islanding and Re-Assessment of Interconnection Requirements in High Penetration of Customer Sited PV Generation

Task 3 Report: Aggregate PV Inverter Islanding Performance Testing

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Version 1.01
July 5, 2016

imagination at work

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Acknowledgments

This research is supported by the California Public Utilities Commission (CPUC) through the California Solar Initiative (CSI) research development demonstration and deployment (RD&D) grant Solicitation 3.

GE Energy Consulting would also like to acknowledge support of Pacific Gas & Electric, GE Power Conversion, GE Global Research, and Itron.

Executive Summary

This report documents the objectives of the experimental work within the project, provides details of laboratory test setup, and describes procedures used to quantify electrical behavior of PG&E distribution loads when supplied by solar PV inverters and islanded (disconnected) from utility supply. The tests were performed using physical PV inverters coupled with the electronically-controlled load in the ~120kW-scale experiments. The PV inverters used in the tests represent the variety of inverters found on PG&E distribution circuits.

The implementation of load is the key innovation of the project – it is a combination of two systems: 1) the transient load model, executing on a standard hardware and software platform of Real Time Digital Simulator (RTDS) to calculate load currents in response to measured voltage, and 2) the power amplifier, constructed from two MW-class power electronic inverters that extracts the calculated current from the power circuit. The PV inverters (units under test) respond to the load current by changing their output voltage, which is then sensed by a load model in RTDS that calculates new values of load currents and passes them to the amplifier that extracts them from the power circuit. This process runs continuously in real time and allows observations of temporal evolution of islanded behavior of PV inverters and load for any desired load model, at any level of penetration, and at any level of reactive compensation.

The load modeling is based on WECC-guidelines that capture dynamic load properties specific to climatic zones and seasons of the year. WECC classifies load by end-uses that include residential and commercial air conditioners, fans, pumps, residential appliances, lighting, computers, etc. WECC utilities have tested the loads for various end-uses and defined the composite load model made up of seven load categories. Our load implementation allows for adjusting the ratio of these categories in the software model instead of making changes to the physical circuit which results in high efficiency of experimental work and allows unprecedentedly comprehensive evaluation of islanding behavior of PV inverters.

The details of our experimental setup, the test plan, and the summary of completed experiments are provided in this report.

Revision Notes

Authors	Date	Rev	Notes
WM	Aug 2016	1.1	Additional pre-publishing edits
JZB	July 2016	1.01	Minor edits
JZB	Oct-Nov 2015	1.0	Original release
JZB	Aug 2015	0.3	Document structure and draft content
AxEy	Jun 2015	0.2	ATS input

Contents

List of Figures vii

List of Acronyms ix

Introduction 1

Facility Overview 3

PV Inverters 4

Islanding Test Circuit 4

Implementation of Controllable Load 7

Load Modeling in RTDS 8

Power Amplifier 21

Measurement and Control System 25

Test Plan 29

Summary of Completed Experiments 41

Bibliography 43

List of Figures

Figure 2-1 Test Facility Overview Diagram 6

Figure 3-1 Composite load model in RSCAD 10

Figure 3-2 Supplying voltage inputs to the RSCAD load model 11

Figure 3-3 RSCAD load model: Motors A through C 12

Figure 3-4 RSCAD load model: Trip Reconnect Logic of Motor A 15

Figure 3-5 RSCAD load model: Constant R, Constant I, Constant P, and Motor D 16

Figure 3-6 RSCAD load model: Current commands delivery to analog output card of RTDS.. 17

Figure 3-7 RSCAD load model: Scaling of current commands from load components 19

Figure 3-8 RSCAD load model: Internal measurements 20

Figure 3-9 RSCAD load model: User interface 20

Figure 3-10 Photographs of hardware: RTDS rack (left) and Amplifier control cabinet with RTDS analog output card installed atop standard controls (right) 21

Figure 3-11 MW-scale electronic load at PG&E Applied Technology Services in San Ramon CA 22

Figure 4-1 Measurement System: Test Engineer's main interface page 26

Figure 4-2 Measurement system: Breaker panel and current transformers..... 27

Figure 5-1 Residential PV inverters installed at PG&E Applied Technology Services Center in San Ramon CA 32

Figure 5-2 Test procedure 33

Figure 5-3 Screen capture documenting load composition choices in RSCAD Runtime and the corresponding power measurements from LabView 34

Figure 5-4 Example “Definitions” sheet – part of the TestLog spreadsheet for Sumer05 load composition 35

Figure 5-5 TestLog spreadsheet for Summer05 load composition 38

List of Acronyms

ATS Applied Technology Services

HVAC High Volume Air Conditioning

MGTF Modular Generation Test Facility

PG&E Pacific Gas and Electric

PV Photo-voltaic

RTDS Real Time Digital Simulator – the hardware product of RTDS Technologies Inc.

RSCAD Software for RTDS – proprietary software used to run RTDS

WECC Western Electricity Coordinating Council

Chapter 1

Introduction

This report documents the details of laboratory test setup and procedures used to quantify electrical behavior of PG&E distribution loads when supplied by solar photovoltaic (PV) inverters and islanded (disconnected) from utility supply. The tests are performed using physical PV inverters coupled with the electronically-controlled load. The implementation of the load is the key innovation of the project – the load is implemented as a combination of transient load model, executing in software, calculating currents in real-time in response to measured voltages, and a separate power-electronic amplifier extracting those currents from the power circuit.

To achieve maximum flexibility, the transient load model is implemented on an industry-proven Real Time Digital Simulator (RTDS) using standard modeling blocks that include: models of passive elements (R, L, C); models of electric machinery (induction machines with user-adjustable parameters); and models of regulated loads – constant current loads representing ballast-controlled fluorescent lightning, and constant power loads representing power supplies of today's electronic equipment in residential uses, and variable-frequency drives in commercial and industrial applications. The RTDS measures circuit voltages in real time and

supplies it to the load model implemented in software. The load model calculates the would-be load currents and supplies these values as analog output signals to the power amplifier that extracts the currents in real-time from a physical circuit. The physical PV inverters supplying the power island respond to currents by modifying their output voltage and the cycle repeats enabling study of transient behavior of realistic utility loads during islanding conditions.

Implementing the load in this way enables streamlined testing since the changes to the load model do not require physical modifications to the circuit – instead, the test engineer simply changes the composition of load from a computer screen and starts a new experiment. The resulting gain in efficiency enables execution of a much greater number of experiments, which enables greater coverage of load diversity in distribution circuits. This enables defining interconnection rules based on test data specific to the load makeup on actual circuits and maximizing the amount of customer-sited PV in distribution systems.

This report describes the details of the experimental setup and is organized as follows. Chapter 2 provides an overview of the test facility and inventories the PV inverters used in the tests. Chapter 3 provides the details of implementation of electronic load including the load modeling in RTDS and the construction of the power amplifier. Chapter 4 provides the details of the measurement system used to capture voltage and current waveforms from the test. Chapter 5 provides the details of the test plan that documents the matrix of tests and its rationale. Finally, Chapter 6 summarizes the completed experiments.

Chapter 2

Facility Overview

All experimental work in this project was performed in the Modular Generation Test Facility (MGTF) at PG&E's San Ramon Applied Technology Services (ATS) Center. This facility has the capability for testing and evaluating distributed generation and storage equipment and their interactions with a utility grid. Overall capabilities of MGTF include:

- 500 kVA facility rating and equally rated switchgear for independent power production
- 3-phase, 480 Volt wye service
- Multiple bus configurations for islanding capability
- Protection for utility under/over frequency, under/over voltage, and ground fault current
- 400 kW variable resistive load controllable in 5kW increments
- 300 kVAR variable inductive load controllable in 3.75 kVAR increments
- 150 kVAR variable capacitive load controllable in 50 kVAR increments
- Natural gas supply
- 70-foot by 40-foot building designed for distributed resource testing

PV Inverters

The facility also includes the fleet of PV inverters powered by controllable DC power supplies. The available inverters are a sample of popular makes and models deployed on PG&E's distribution system. The summary of available units is provided in Table 2-1. Vendor names and model numbers are obscured by unit codes for privacy.

Table 2-1 List of PV inverters available at PG&E's Applied Technolgy Services Center in San Ramon CA

Unit Code	Number of Phases	Number Available	Maximum AC Output (kW)
x100	3	1	75
x45	3	1	42
r4kW 120Vac	1	4	4
r4kW 240Vac	1	10	3.8-4
r3.3kW 240Vac	1	6	3-3.3
r2.5kW 240Vac	1	10	1.5-2.5

The maximum concurrent output of the installed inverter fleet is 140kW; limited by the capabilities of their DC power supplies and the need to balance the total generation over three phases to match the 3-phase electronic load.

Islanding Test Circuit

The simplified circuit diagram of the test circuit is shown in Figure 2-1. Starting from the left, there is a connection to PG&E 480V service which powers the DC power supplies of the PV inverters. Another connection to the same 480V service is made on the other side of the

diagram via the islanding circuit breaker (CB.) From top to bottom, the equipment shown between the two 480V rails includes:

1) A three-phase DC power supply powering two three-phase PV inverters. Each is interfaced via a dedicated step-up transformer to the 480V bus on the right-hand side.
2) Below it, there are three groups of residential PV inverters. Each group consists of multiple power-supply/inverter pairs connected together on the AC side and interfaced to the 480V bus using a single phase transformer dedicated to the group.
3) Shown near the bottom is the electronically controlled load. From left to right there is an isolation transformer, the three phase power supply, and the three phase power-electronic amplifier controlled by the signals from RTDS.

The islanding tests are performed by bringing up the equipment to the desired operating point and then opening the circuit breaker CB to create the electrical island. This forces the output of the PV inverters to flow into the electronic load and enables observation of transient values of voltages and currents from the initiation of islanding up to its cessation. The tests are orchestrated and recorded using the custom-built data acquisition system (DAS) based on National Instruments' PXIe-1062Q Express Chassis and programmed in LabView. This system is symbolically shown as a blue rectangle labeled LabView. The signals from current and voltage transformers recorded by the DAS are designated by blue lines in the diagram. Note that the voltage signals from the island are also supplied to RTDS to allow execution of the load model in response to actual circuit voltage.

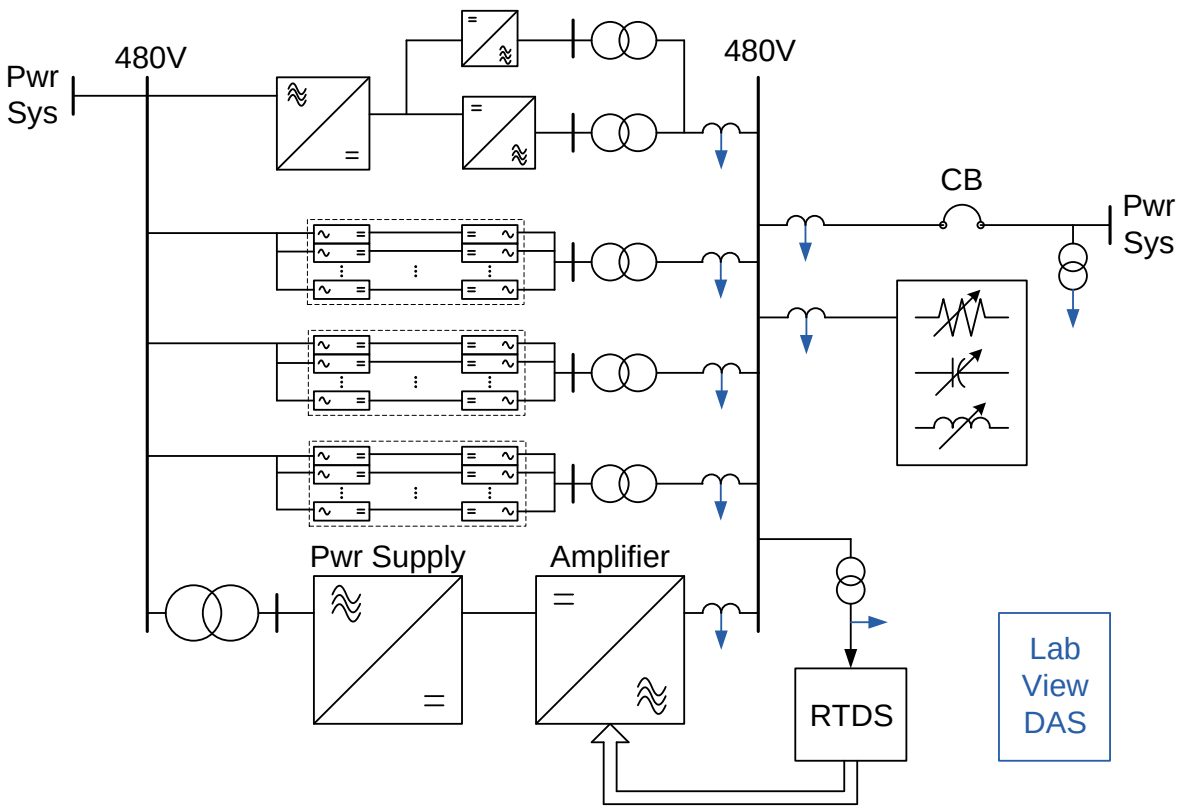

Figure 2-1 Test Facility Overview Diagram

The passive adjustable load, shown below CB, was used in characterization of the amplifier during commissioning of the test and to reduce capacitive current of the amplifier during testing.

Chapter 3

Implementation of Controllable Load

The electronically controllable load is the key enabler of comprehensive study of behavior of utility loads supplied by PV inverters during islanding conditions. Utility loads consist of a large variety of devices – from the simplest: such as resistance found in heating elements and incandescent lightning, to more complex: including many varieties of motors, fluorescent lights, and power supplies used in computers and modern appliances – the loads exhibit different behavior in response to voltage and its collective interaction with PV inverters will vary depending on the actual load composition. At the same time, for sake of practicality, the ability of inverters to detect islanding is evaluated in type-tests using a synthetic load based on the parallel combination of RLC. As a result, the utility engineers charged with defining interconnection rules have little information applicable to realistic scenarios in the field where loads have greater variety than the RLC circuit used in the anti-islanding tests and PV inverters involve different models and sizes from different vendors, possibly causing unanticipated interactions between their active anti-islanding algorithms.

To address these challenges and enable comprehensive evaluation of impact of load on islanding transients, we generalized load modeling by dividing it into two parts:

1) the model of arbitrary load implemented in Real Time Digital Simulators (RTDS) responsible for calculating would-be load currents in response to system voltage, and
2) the power amplifier receiving calculated load currents and extracting them from the power circuit.

These two functional blocks are described in the following sections.

Load Modeling in RTDS

The load modeling used in this project follows WECC guidelines described in [1]. The guidelines are a result of decades of work by WECC utilities aimed to capture dynamic load properties specific to 12 climatic zones – a function of region, and 5 seasons of the year – three for summer (normal, peak, cool), one for shoulder season, and one for winter. Within each group the load is classified by end-use including residential and commercial air conditioners, fans, pumps, residential appliances, lighting, computers, etc. WECC utilities have tested the loads for various end uses and proposed the composite load model made up of seven load categories: 4 types of motors, Static R (incandescent lighting, electric water heaters, space heaters), Static I (ballast-controlled fluorescent lighting), and power electronic loads (electronic power supplies, and variable speed drives)

Our study from phase 2 of this project [2] analyzed three load zones of PG&E in different climate zones and applied composite load modeling guidelines to the study of distribution system loads. The work in [2] analyzed over 500 distribution circuits to the level of sections and mapped the actual load in the sections to the load compositions for summer and winter, resulting in the total number of 3,440 compositions. These compositions were then clustered

and clusters prioritized by frequency of occurrence. Each cluster yielded the average composition and the prioritized list of average values by cluster became the input to the experimental stage. The inputs are supplied to the load model in RTDS in the form of percentage blend between different components of load. For example, an ordered seven-tuple (0.211, 0.102, 0.224, 0.132, 0.097, 0.179, 0.054) means to blend 21.1% of Motor A, with 10.2% of Motor B, with 22.4% of Motor C, and so on.

The high-level organization of the composite load model in RSCAD is shown in Figure 3-1. The complexity of this figure makes it impractical for description – the main point of including it is to provide a visual map of interconnection between different functional blocks. The main functional blocks include:

1) Input of circuit voltage from analog input channels of RTDS and their routing to models of voltage sources supplying the load models
2) Load models including three motor models, the ZIP model, and the functional model of air-conditioning load.
3) Delivery of output currents from the model to the analog output channels of RTDS, including appropriate scaling to account for the desired percentage composition of different load components.

These functional blocks are reviewed in detail with reference to their relevant parts of the diagram provided as separate figures.

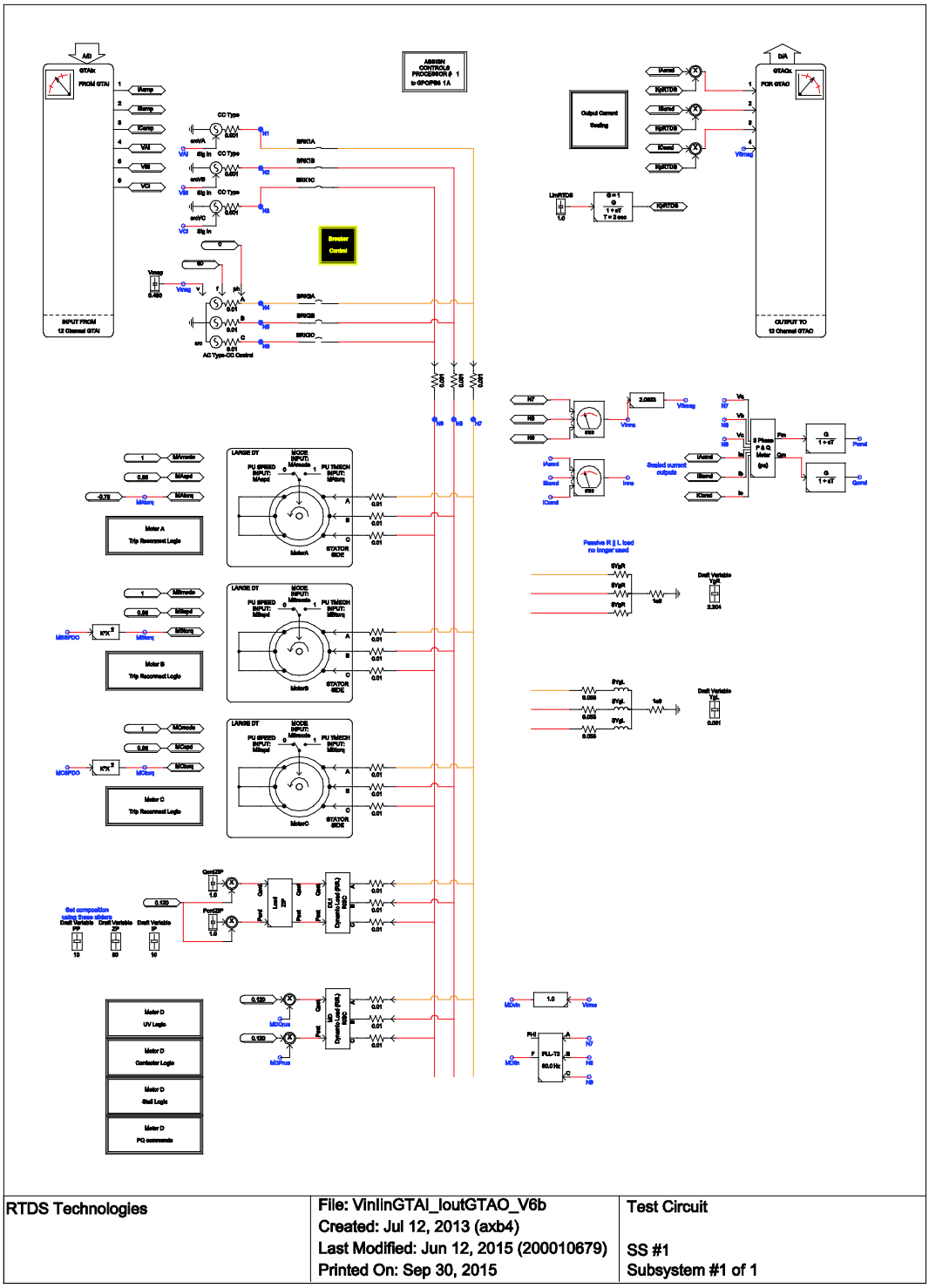

Figure 3-1 Composite load model in RSCAD

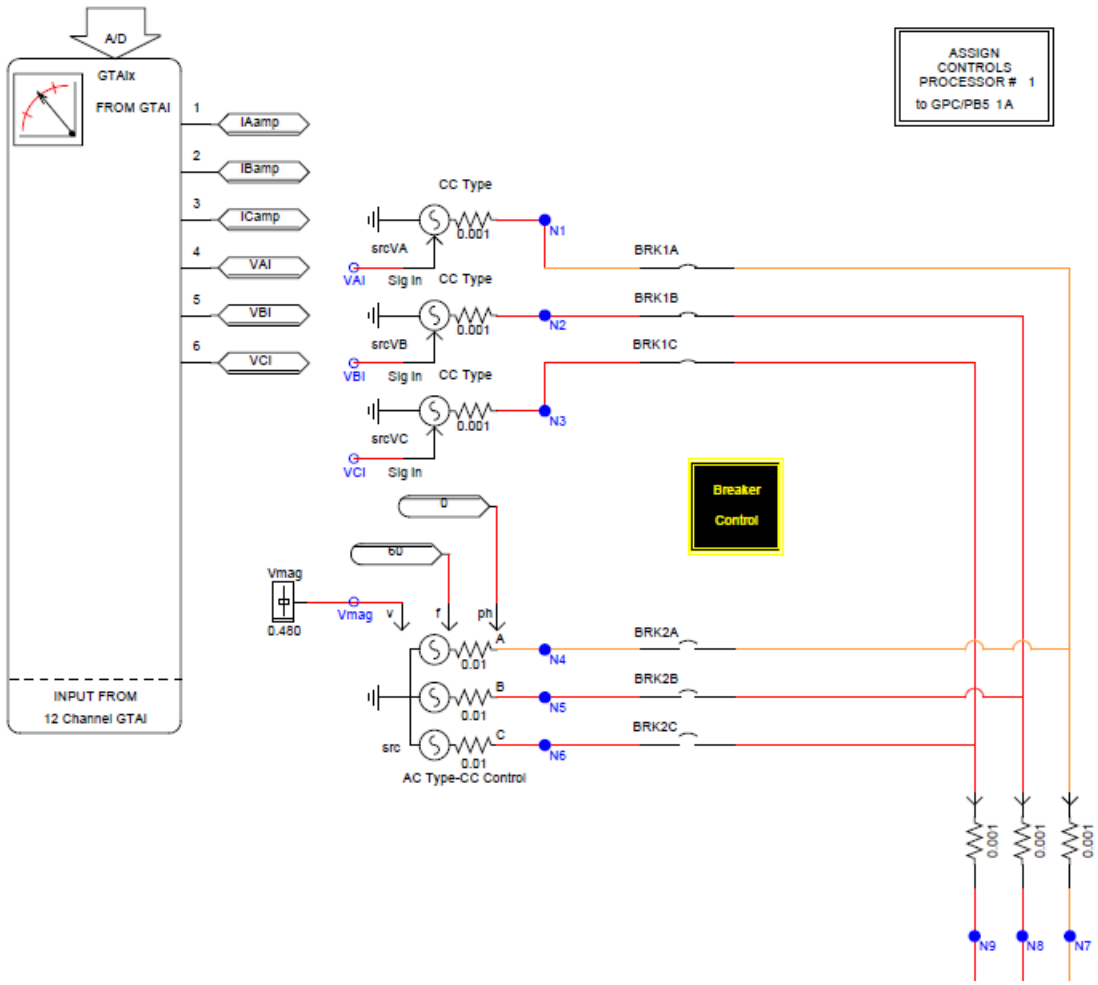

Figure 3-2 Supplying voltage inputs to the RSCAD load model

The first functional block is shown in Figure 3-2, documenting the voltage inputs to RSCAD load model. A standard RSCAD block is used to deliver signals from the analog input card to the simulation and the analog input signals are used to define instantaneous voltages of controllable voltage sources. The measured voltages from the power system effectively become applied to the circuit model within RSCAD at nodes N1-N3. Below this block is an alternative set of voltage sources using ideal sinusoidal voltages defined in magnitude by the user adjustable variable Vmag (from the slider), and fixed frequency of 60Hz with phase angle 0. This alternative set of sources was useful in characterizing components of the load model and

troubleshooting logic for modeling motor stall and recovery characteristics. The selection of the applicable source of voltage is performed using the “Breaker Control” block shown between the two circuits.

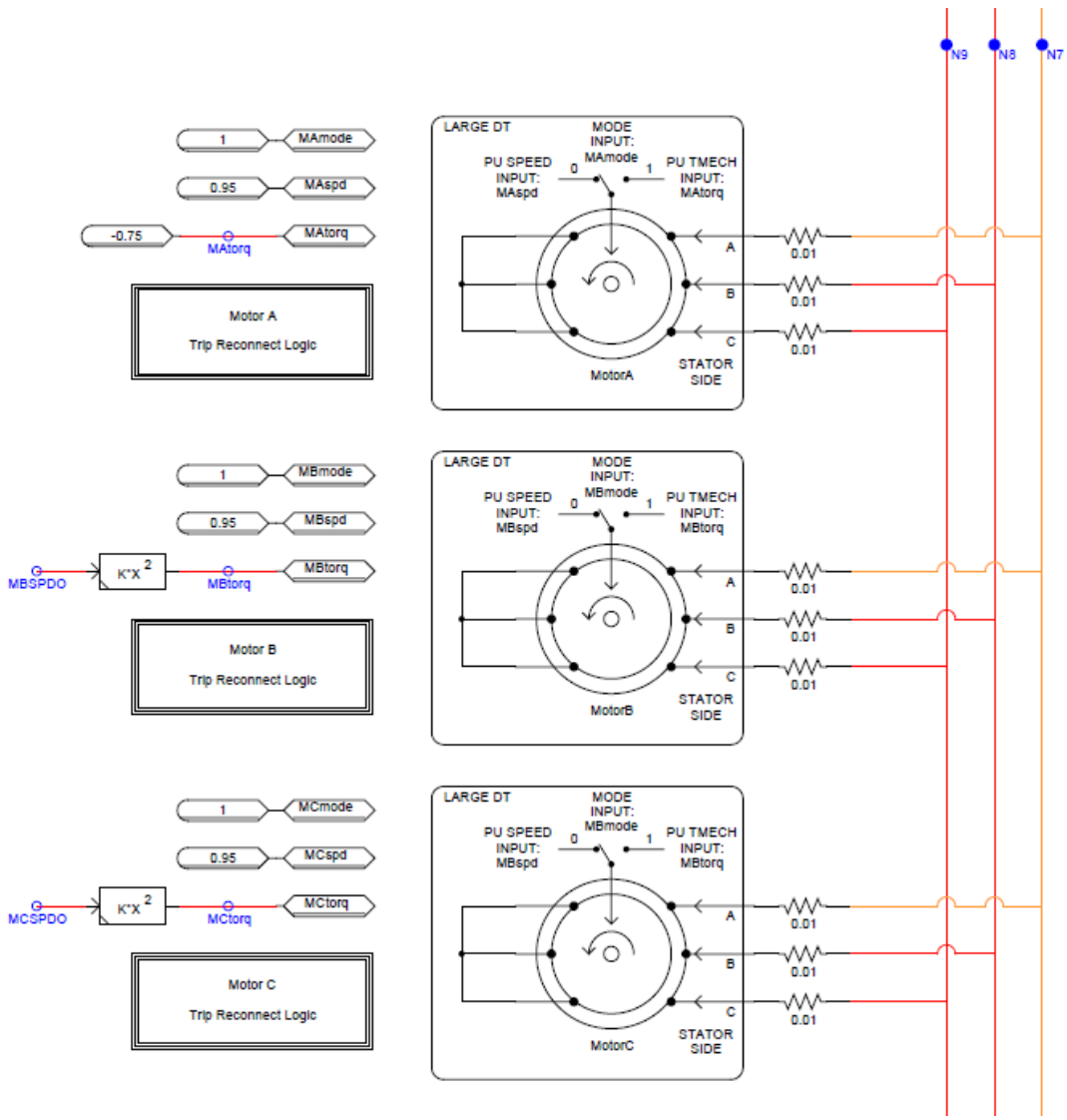

Figure 3-3 RSCAD load model: Motors A through C

The second functional block is shown in Figure 3-3. RSCAD’s standard library model of an induction motor is used to interface with the power circuit, but each one is parameterized differently to account for different motor properties of motor types in the composite load

model. The parameter values are too numerous to include here; they can be obtained from the RSCAD file that accompanies this report. The composite load model uses Motor A to represent compressors used in refrigeration. This is accounted-for by setting the load torque to a fixed value. Fixed value in this context means independent of speed while the value of 0.75pu represents the presumed average loading of motors employed in refrigeration (a WECC recommendation). In contrast, the torque value for Motors B and C is a quadratic function of speed, because Motor B represents fans and Motor C pumps. Each motor model is accompanied by an additional control block which defines WECC-recommended aggregate behavior of the corresponding motor type relative to voltage. For example, refrigeration motors (Motor A) will trip if their voltage is below a certain threshold for more than a certain amount of time. After that, some motors will stay off until they are restarted by a user, and some will restart automatically if the voltage recovers. The WECC-recommended practice is to assume that 20% of the motors will trip if the voltage is below 0.7pu for more than 20ms and stay off permanently. The other 70% of motors will trip if the voltage falls below 0.5pu for longer than 20ms, but this group will restart if the voltage recovers above 0.7pu for longer than 100ms.

This behavior is implemented using a control block diagram shown in Figure 3-4. Discussing details of this implementation is beyond the scope of this document, but we do offer a high-level overview to aid an interested reader. There are three parts to the diagram: the two shown on the left-hand side are managing trip-reconnect logic for the two sets of thresholds, while the third one, shown to the right, blends the output into a multiplier coefficient delivered back to the main page of RSCAD model. The structure of the trip-reconnect logic is the same for two groups, but the thresholds and time delays are set at different values. Measured voltage

magnitude “VSmag” is brought into the diagrams as an input signal and compared to the relevant voltage thresholds in the comparator blocks. The thresholds are set as user-adjustable constants, set to correspond to WECC-recommended values. The outputs of voltage comparators are routed by the switches controlled by the state of the group. If either threshold condition is active, the corresponding timer starts and it ultimately effects the state change of its downstream comparator when the accumulated time becomes greater than the corresponding time delay constant. The first group (shown at the top) never recovers from an under voltage condition, so there is a pushbutton input “TRLrst” that resets the logic. The states of the two groups are encoded into a multiplier coefficient “MAmult”, which is the ultimate output of the control diagram used to multiply the Motor A currents that are summed into current references for the amplifier. More on that is discussed with reference to the corresponding diagram from the main page.

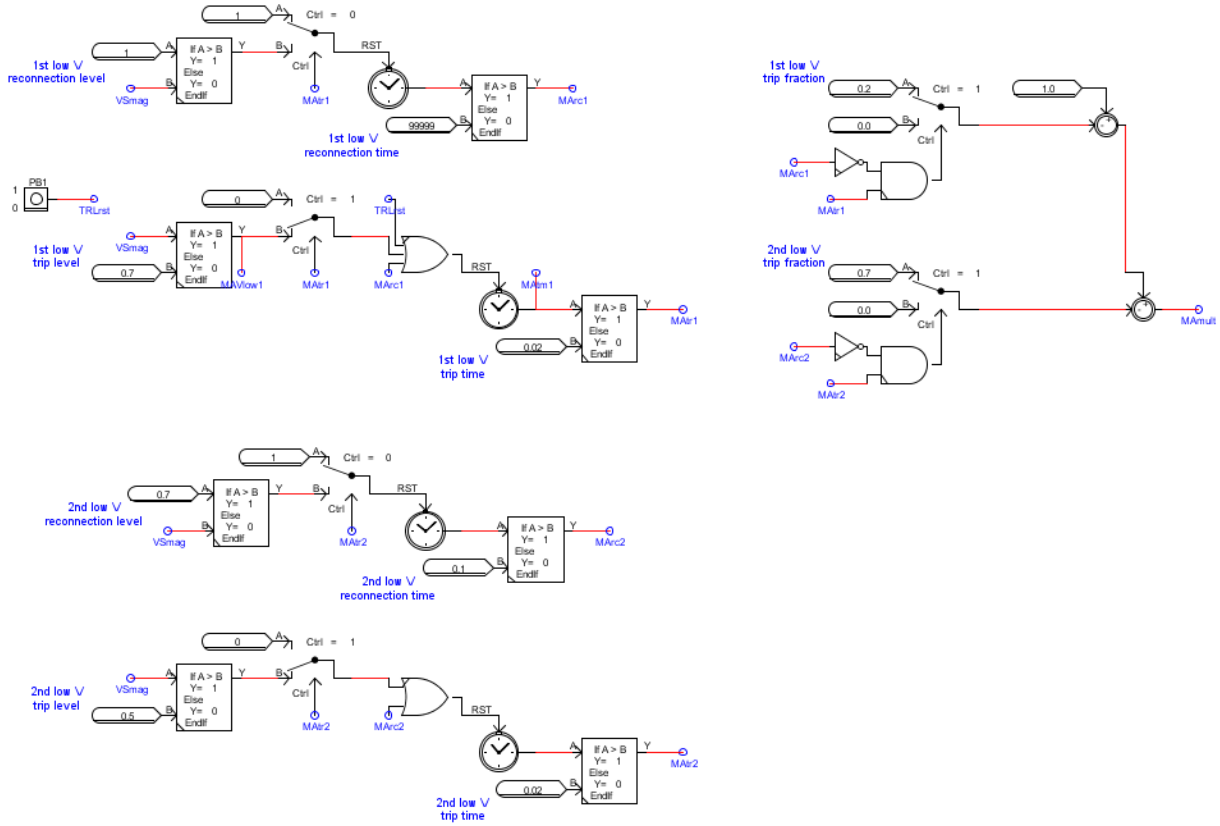

Figure 3-4 RSCAD load model: Trip Reconnect Logic of Motor A

Referring back to the main diagram, the third functional block is shown in Figure 3-5. There are two parts to it: the ZIP load implementation shown in the top part of Figure 3-5 and the Motor D model, shown in the bottom, which is a functional model of air-conditioning loads implemented per WECC recommendations. Both loads leverage the standard Dynamic Load component of RSCAD as a circuit interface and use upstream blocks to provide P and Q set-points. In the case of ZIP load (implementing the functions of Static R using constant impedance "Z", Static I using constant current "I", and Power Electronics using constant Power "P") the functionality is achieved by leveraging another standard block from RSCAD library: "Load ZIP", while the functional model of Motor D is coded into four control diagrams.

The use of Dynamic Load component to extract the current from the circuit based on P, Q set-points may appear risky in terms of stability because regulating power extraction from a declining voltage requires increase in current to keep P and Q constant (on the account that P and Q are proportional to the product of current and voltage.) However, it should be noted that the P and Q set-points are not held constant in this implementation – they are dynamically adjusted by the upstream blocks in response to the varying voltage. As a result the system of blocks self-regulates through a wide range of voltage[1].

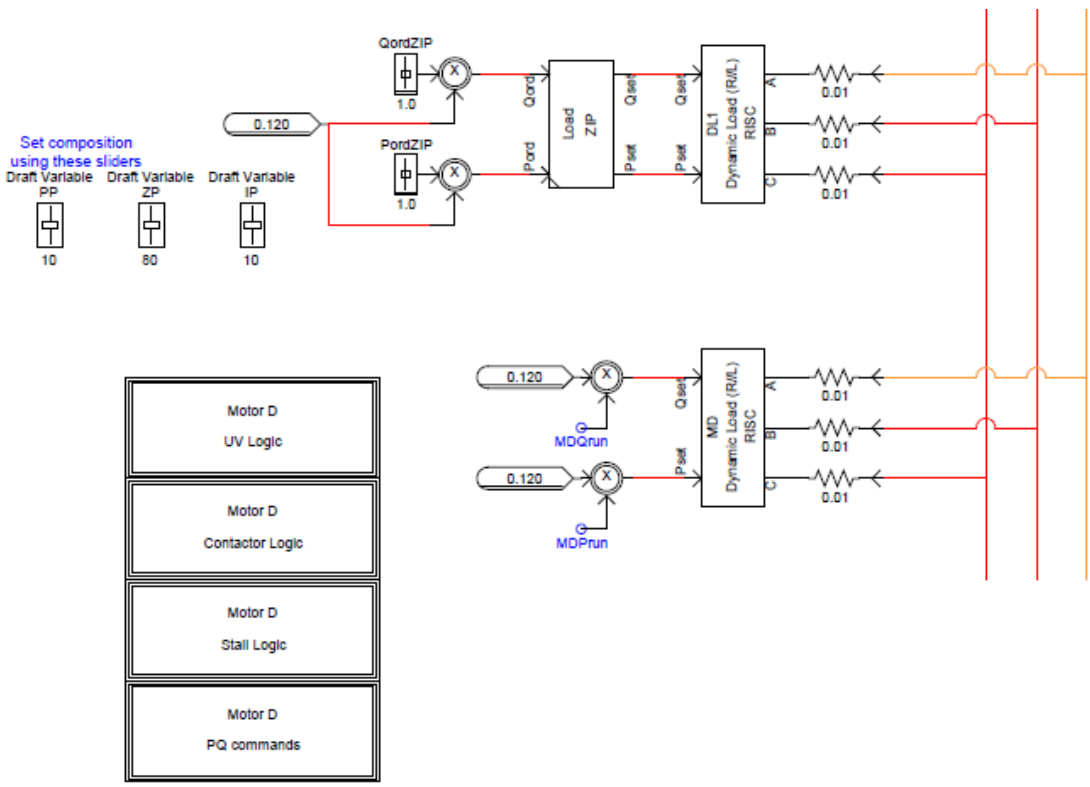

Figure 3-5 RSCAD load model: Constant R, Constant I, Constant P, and Motor D

The next functional block diagram is shown in Figure 3-6. Current commands, prepared in the sub-block named "Output Current Scaling", are delivered as signals to the standard RSCAD

[1] The Dynamic Load component also has internal safeguards turning it into equivalent impedance below 0.5pu voltage

block that handles the digital to analog output and RTDS hardware takes care of the rest. Note that commands are multiplied by a signal “KpRTDS” which is generated by low-pass filtering the user input “LimRTDS”, originating on the slider component. The purpose of this signal is to allow slow application of analog outputs from RTDS to the amplifier – useful in troubleshooting. By setting “LimRTDS” to zero, a test engineer can operate the load model and inspect the current signals without applying them to the amplifier. When satisfied with the output, the test engineer can simply enter the value of 1 into LimRTDS and the low pass filter applies the change gently to the amplifier. The signal is also used for fine adjustments of total load power to achieve target penetration level as will be discussed in Chapter 5.

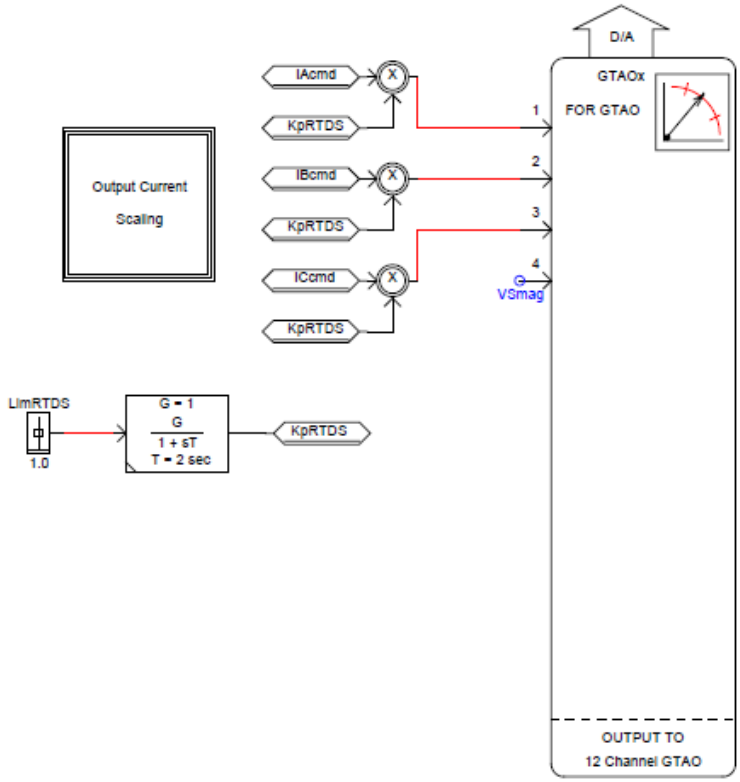

Figure 3-6 RSCAD load model: Current commands delivery to analog output card of RTDS

The implementation of “Output Current Scaling” is shown in Figure 3-7 for the signal “IAcmd” (identical implementations are applied for scaling current commands of the other two phases). The non-obvious part of the implementation is the meaning of scaling signals. Referring to the signal path of Motor A, i.e. starting by the signal named “MAISA” – the scaling constant “MApu” designates the relative content of Motor A within the composite load model. This enables configuring the circuit model of Motor A to be rated to a nominal value of the load and blending its content into the total output using a scaling coefficient adjustable from the RSCAD runtime screen without the need to recompile the load model. The “MAmult” follows and applies additional scaling due to Motor A’s trip-reconnect logic discussed in reference to Figure 3-4. The meaning of signals is identical for Motors B and C. Motor D is different in that it has a more complex logic, the effects of which get incorporated into P and Q references of its Dynamic Load model. As a result, the current signal MDISA has the effects of scaling already built in, making it unnecessary to apply the second multiplier. Nonetheless, the signal path in Figure 3-7 is left to be structurally the same as other paths, but the second multiplier is effectively disabled by setting the multiplication signal to a constant value of 1. The implementation of scaling of ZIP outputs is analogous to the one of Motor D, but in this case, the incoming signal of current “ZIPIA” embodies the scaling for blending relative content of ZIP within the load composition, and there is no applicable trip-reconnect multiplier resulting in both multipliers in Figure 3-7 to be set to 1.

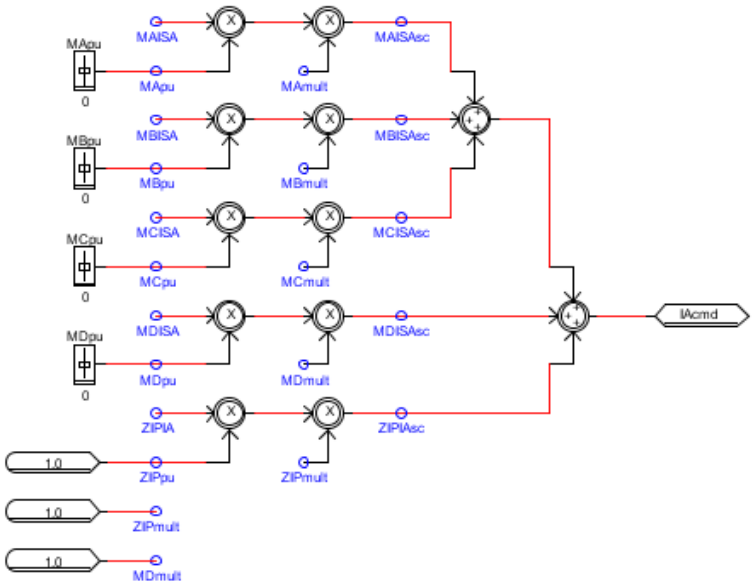

Figure 3-7 RSCAD load model: Scaling of current commands from load components

Referring back to Figure 3-5, the relative content of Static R, Static I, and Power Electronic load within ZIP model is chosen using slider components shown next to the ZIP load model.

The final functional block of RSCAD load implementation is implementing measurements of electrical quantities within the load model shown in Figure 3-8. These measurements enable:

a) Operation of trip-reconnect logic of motors via “Vsmag”, and

b) comparison of active and reactive power drawn by the model with active and reactive power drawn by the physical load. These values are captured during tests for purpose of quality assurance.

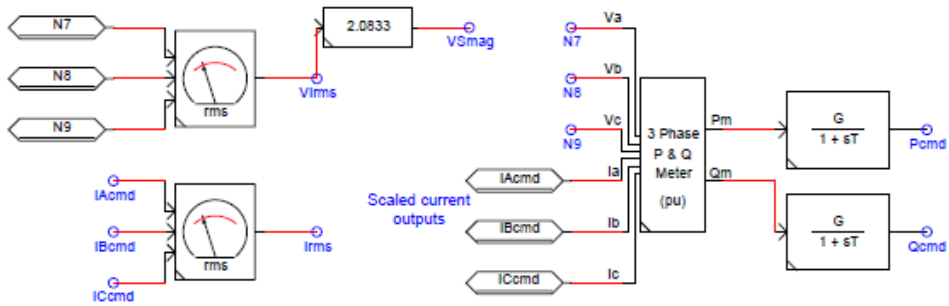

Figure 3-8 RSCAD load model: Internal measurements

The user interface to the RSCAD load model is shown in Figure 3-9. The group of sliders in the middle of the figure configures the composition of various components of the load. The waveform displays and other instruments are aiding the test engineer in establishing that the test conditions are as expected – another aspect of quality assurance.

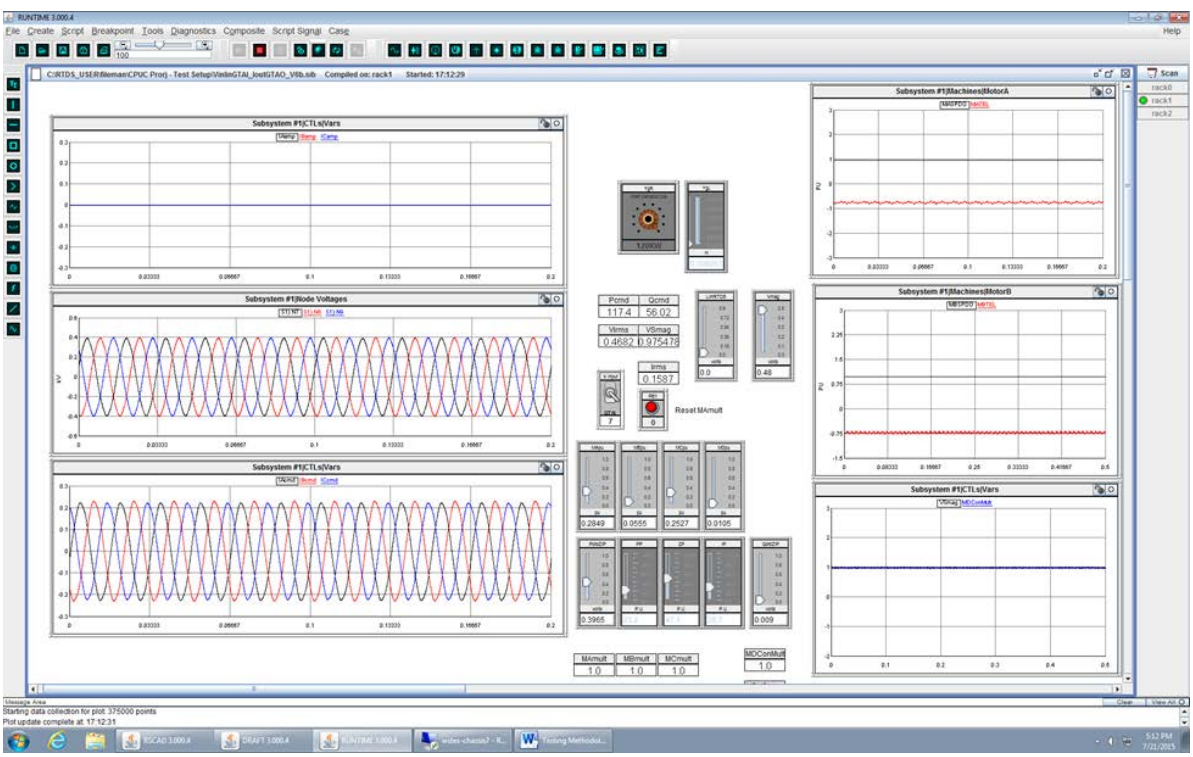

Figure 3-9 RSCAD load model: User interface

Finally, the photograph of the RTDS rack (located inside MGTF) and the integration of RTDS analog output card within the control cabinet of the Amplifier (located outside MGTF) are shown in Figure 3-10. Locating the RTDS analog output card within the amplifier control cabinet minimizes the noise pickup on the signals. The card is referenced to the same analog ground as other control cards within the amplifier and connected to RTDS via a fiber optic cable.

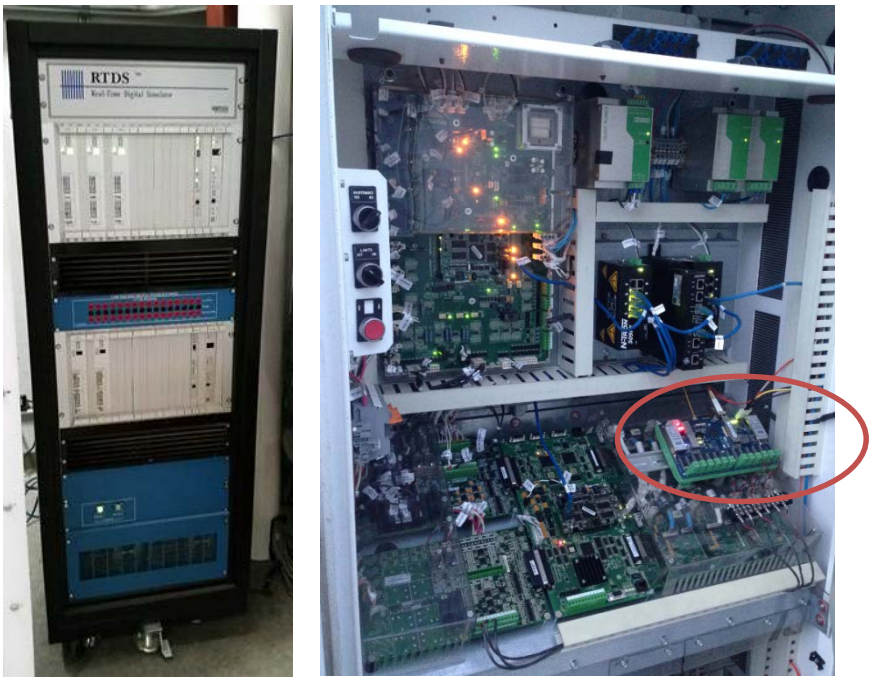

Figure 3-10 Photographs of hardware: RTDS rack (left) and Amplifier control cabinet with RTDS analog output card installed atop standard controls (right)

Power Amplifier

The electronic load was built using two utility scale solar inverters connected back to back to exchange power via a DC circuit (normally used to connect PV panels). The photograph of the two units as installed in PG&E ATS facility is shown in Figure 3-11. One inverter, acting as a power supply, has its AC terminals continuously connected to the utility voltage via an isolation

transformer. It is operated to control the voltage on the DC connection between the two units. The other one, acting as a current amplifier, has its AC terminals connected to the bus that gets islanded. The nameplate ratings of the two units are 750kW[2] for the power supply and 1MW for the amplifier. However, since the total simultaneous capability of PV inverters used in the test amounts to 140kW, the amplifier was modified to be rated to 250kW, one quarter of its design ratings. Operating a unit at a de-rated power output is advantageous from the standpoint of control bandwidth, but disadvantageous from the standpoint of accuracy of its built-in measurement systems. This was overcome by replacing bridge current sensors to lower their range to one quarter of original value.

Figure 3-11 MW-scale electronic load at PG&E Applied Technology Services in San Ramon CA

The primary control objective of the amplifier is high-speed closed-loop control of current. In the process, the unit must cancel the current flowing through its own harmonic filter, which includes a capacitance directly connected to the AC line voltage. The role of this capacitance in

[2] The power supply uses the same power electronic bridge as the 1MW unit, but allows for a greater reactive output range which comes at the expense of active power rating

normal operation is to provide the path for inverter-generated current harmonics. However, as a harmonic sink, it also attracts grid harmonics. This is not a significant issue in normal applications because absorbing the harmonic currents from the grid helps control harmonic voltage levels near the equipment, but it becomes an issue in amplifier application where the current exchanged with the grid needs to be nulled unless requested by the load model. This was a daunting task. Getting acceptable results required disconnecting one half of the AC harmonic filter capacitance to reduce the grid harmonic current flow through the filter, and repurposing of current feedback signals from measuring total output current of the unit to measuring current through the AC capacitance so that it can be directly controlled by the firmware.

Other modifications included operating the internal chopper using only one phase of a three-phase bridge to indirectly increase the resolution of current measurement on the DC side by forcing the DC current to flow through one leg of the chopper instead of three which effectively triples the measurement resolution.

The control firmware was completely rewritten for this application and comprehensively evaluated for closed-loop accuracy of tracking current references from RTDS. The overall current control system does inevitably have implementation latency associated with the following time delays:

1) Signal acquisition by A/D converters of RTDS
2) Signal transfer from analog I/O card to the CPU
3) Execution of the load model

4) Signal transfer of calculated current signals to the D/A card
5) Signal output by D/A converters
6) Sampling of analog input by the control system of the amplifier
7) One step calculation delay in the amplifier
8) Output via PWM of the power electronic bridge in the amplifier

Steps 1-5 are executing at the time step of RTDS (10µs), while steps 6-7 are executing at the switching frequency of the inverter (5856Hz, ~171µs) dominating the overall latency. The resulting error manifests itself as a phase angle delay of current and can be quantified by operating the amplifier using a purely resistive load model and measuring the resulting power factor of the load current in the power circuit. The error was quantified and compensated by advancing the current references within the amplifier to compensate for the phase shift. Since the control implementation is digital the latencies are known and fixed, so compensating for the error is a one-time adjustment.

Chapter 4

Measurement and Control System

As was mentioned in Chapter 2, the measurement system used in the experiments is based on National Instruments' "PXIe-1062Q Express Chassis" and programmed in LabView. The same hardware orchestrates the tests – it operates the islanding contactor and several other switches that can be used to isolate groups of equipment and triggers the data acquisition and recording of test results into files. The main control screen for the test is shown in Figure 4-1. To the left of "Island Bus", is a control switch for the islanding contactor – shown in closed position (designated by red color.) To the right are four additional remotely operated switches used to energize different groups of PV inverters. "Bay 1" has three load centers, each connecting a group of single-phase PV inverters. The transformers connecting groups of single-phase inverters (shown in Figure 2-1) are connected line-to-line on the 480V side (important for correct summation of their corresponding CT signals into phase currents). "Bay 2" connects the three-phase inverters, "GE Load" designates the power-electronic amplifier, "RLC load" designates the step-wise adjustable load banks. The phase currents supplied or consumed by different equipment groups are monitored by current transformers and their instantaneous values tracked by the measurement system.

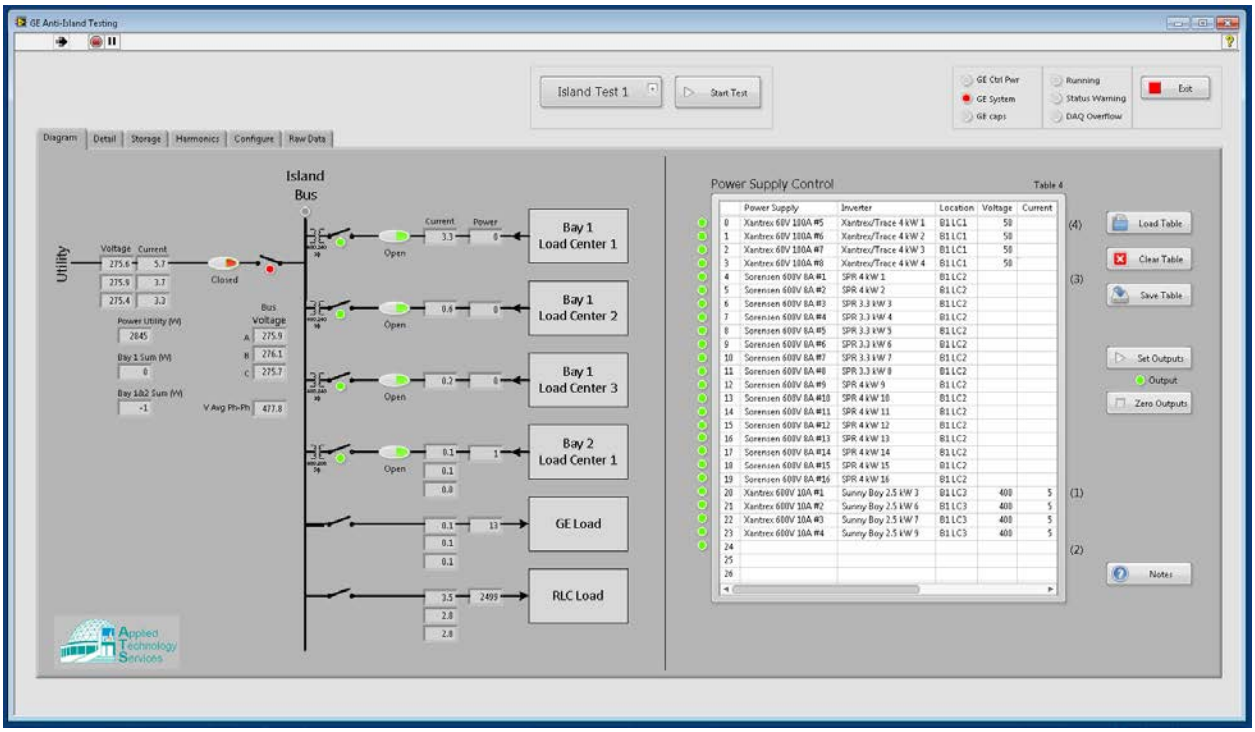

Figure 4-1 Measurement System: Test Engineer's main interface page

A photograph of the breaker panel with side panels removed to expose current transformers is shown in Figure 4-2.

The measurement system also tracks instantaneous values of phase to neutral voltages of the grid (upstream from the islanding contactor,) phase to neutral voltages of the island, and line currents of the grid, using potential and current transformers (not shown in Figure 4-2). The RMS values of voltages and currents and the corresponding values of active power are continuously calculated by the custom LabView code and streamed to the main page with 1 sec update-rate to provide quantitative feedback to the test engineer.

Figure 4-2 Measurement system: Breaker panel and current transformers

The test configuration has considerable flexibility which was of great help during system commissioning. Example use-cases exercised during system commissioning follow.

1) The system is energized to apply voltage signals to RTDS and enable characterization of load models in response to non-ideal grid voltages.
2) Each PV inverter group runs directly connected to the grid to characterize its maximum output capability.
3) Combinations of PV inverter groups run connected to the grid to evaluate if harmonic or control interactions are of concern.

4) The amplifier runs connected to the grid to enable its tuning and characterization.
5) Islanding tests are performed using PV inverters and passive loads to establish their baseline behavior.
6) Islanding tests are performed using PV inverters and the amplifier.
7) Islanding tests are performed using passive loads in addition to the amplifier to offload a portion of amplifier loading.

Additional screens (not shown) accessible via tabs from the same user interface provide oscillography functions on the signals, measurements of power and reactive power coupled by different equipment groups, and harmonic content of signals.

The execution of the islanding test sequence is programmed into the tool – after a user-issued command to start the test, the system begins recording of all analog channels into a file, opens the islanding contactor and continues to record until either a specified recording time is reached, or until voltage falls under a specified threshold. The recording time and the voltage threshold are user choices as well as the file name and test comments. The default file names are assigned from an increasing number sequence and include the date and time code of the test. The recordings are saved as binary files in the native LabView format, which includes data describing the configuration of input channels (e.g. scale, offset, sampling frequency) and the raw recordings. The only drawback of the tool is that it saves multiple files per test, so the recordings have to be concatenated in post-processing to obtain results for the full duration of the test.

Chapter 5

Test Plan

As was discussed in [2], the main objective of this project is to improve the understanding of the combined behavior of PV inverters and connected loads in the interval of time from occurrence of islanding to its eventual cessation. We are seeking to find and evaluate conditions that make islanding detection difficult and to capture the resulting voltage and frequency during these conditions in laboratory measurements. In doing this, we are interested only in realistic conditions – those that are likely to occur on real distribution circuits with realistic load varieties.

The work described in [2] assessed the diversity of load compositions on a statistically representative sample of PG&E circuits. The seven-dimensional space of load compositions was then prioritized based on frequency of occurrence to prioritize laboratory evaluation. Next, the controllable load was built as described in Chapter 3, to enable efficient evaluation of different load compositions. The load composition is adjusted by adjusting sliders in RTDS instead of making changes to the power circuit, providing critically important efficiency of testing process.

The remaining variables of interest are the level of reactive compensation on the circuit section, and the level of PV penetration. These selections are orthogonal to one another and to load

compositions, meaning that any number of choices for reactive power factor will multiply the number of choices for PV penetration then multiply the number of choices of load compositions, resulting in combinatorial expansion in number of experiments. This was given careful consideration by the project team, and it was ultimately decided to consider four choices of reactive compensation and five levels of PV penetration. The rationale is provided in the following paragraphs.

For reactive compensation we chose power factors of: 0.95 inductive, 0.98 inductive, 1.0, and 0.98 capacitive. These choices are prudent because PG&E is quite vigilant about reactive compensation of its distribution circuits – in the three load zones we studied the average number of reactive compensation capacitors per feeder is ~4.6. It is therefore likely that an islanded section of a distribution circuit will operate at a power factor close to unity and exploring the range between 0.95 inductive and 0.98 capacitive covers all likely options.

There are two ways to achieve different penetration levels of PV: One is to hold the load constant and vary the output of PV units; another to set the PV output to a constant value and vary the load. The first option (to hold the load constant and vary PV) makes the installation less costly – the cable and switchgear ratings for amplifier connections need to match the installed PV, not surpass it to accommodate the minimum level of penetration. For example, reaching 30% penetration by varying the load on a total of 140kW of PV generation, would require wiring the load to support 466kW. In contrast, varying the PV on a fixed load requires sizing the load to match the maximum output of PV plus the desired range of reactive loading. We chose the first option: to vary PV on a fixed load. The test setup at ATS was wired for

250kVA, which allows for ample reactive range around the maximum available PV output of 140kW. The PV output was then varied by varying the number of PV inverters in service. When in service, the inverters were operated at their maximum attainable AC output. Figure 5-1 shows the so-called “wall of inverters” installed at PG&E’s ATS. Each inverter has a dedicated power supply (installed in racks behind the wall) and it is connected or disconnected from the test using panel breakers installed within breaker boxes (visible in the photograph to the right of each inverter group). The color-coded switching map is visible next to the panel doors – it guides the test engineer in selecting which units are in service for a specific test condition.

The residential units were grouped into four configurations resulting in different levels of power output. Table 5-1 documents these configurations in order of descending power output, and introduces letter codes: “d” through “a” used to designate them. The equipment used for each configuration is listed in table columns under each letter code. Each row of the table corresponds to one type of available PV inverters and the table cells document the power output from the corresponding types of units and the number of units used in the test. For example, configuration “d” gets 24kW of PV generation from 6 PV inverters of “r4kW 240Vac” type; designated by 24 (6) in the corresponding table cell.

Figure 5-1 Residential PV inverters installed at PG&E Applied Technology Services Center in San Ramon CA

Table 5-1 Groupings of residential inverters in different test configurations

Configuration Code	d	C	b	a
r4kW 120Vac	16 (4)	16 (4)	16 (4)	12 (3)
r4kW 240Vac	24 (6)	20 (5)	16 (4)	12 (3)
r3.3kW 240Vac	16 (5)	13 (4)	10 (3)	7 (2)
r2.5kW 240Vac	10 (4)	5 (3)	5 (3)	5 (3)
Total Power (kW)	**66**	**54**	**47**	**36**

Using these configurations individually or combining them with either of the three-phase units (x45 and x100) allows for twelve possible values of PV power output and, consequently, twelve

possible values for % penetration assuming that the load is held constant. The team has ultimately chosen five levels of penetration designated by: “`xoff b`”, “`x45 a`”, “`x45 c`”, “`x100 b`”, “`x100 c`”. Holding the load constant at 120kW these combinations of PV inverters results in levels of penetration of: 36%, 61%, 80%, 100%, and 108%, respectively.

The complete set of steps of the test procedure is shown in Figure 5-2. The test procedure is a group of nested loops that alternate test configurations. We represent it using a color-coded set of steps where related steps are shown in the same color and related repetition described in words. The resulting visual is, we feel, more compact and therefore more readily absorbed than an equivalent flow-chart. A brief description of the steps follows.

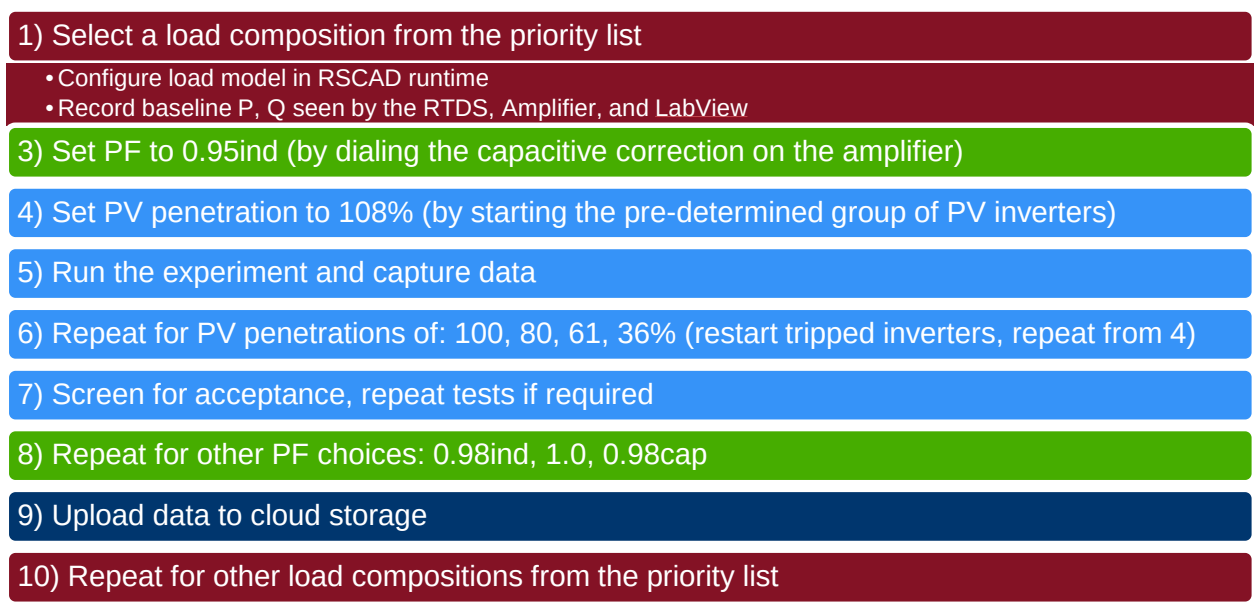

Figure 5-2 Test procedure

First, a load composition is selected from the priority list and the corresponding load model is configured in “RSCAD runtime” using the interface shown earlier in Figure 3-9. As a part of the

quality assurance process, the test engineer captures a screen image that documents the selected position of sliders in RSCAD and the screen from LabView that documents the corresponding power of the amplifier and utility. An example screen capture is shown in Figure 5-3.

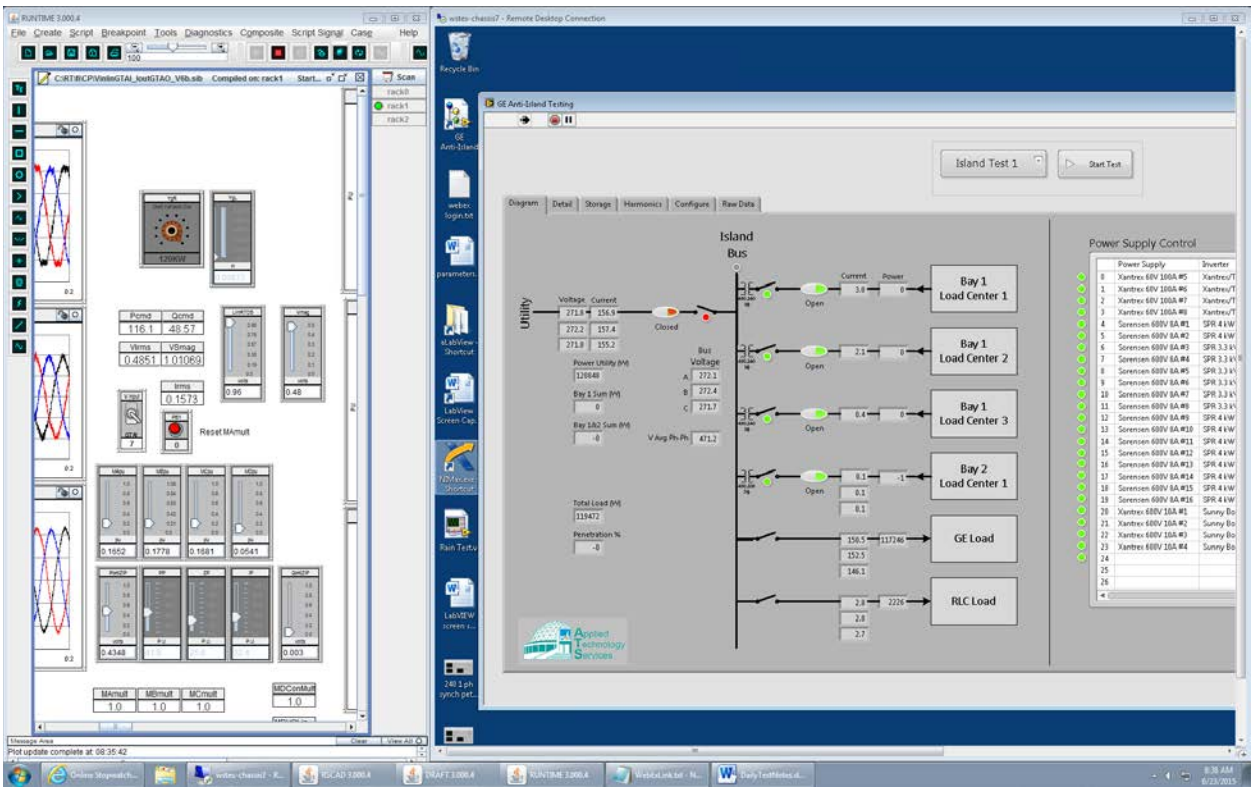

Figure 5-3 Screen capture documenting load composition choices in RSCAD Runtime and the corresponding power measurements from LabView

At this point, the load runs connected to the grid and the resulting values of load's active and reactive power are recorded from all measurement sources for quality assurance. The measured values are entered into the "Definitions" sheet of a "TestLog" spreadsheet. An example Definitions sheet is shown in Figure 5-4. Note that these measurements correspond to inherent load, i.e. load without additional reactive compensation. The use of these measurements will be discussed in the context of TestLog spreadsheet later in this section.

119.6	Utility P [kW] // read from LabView screen
45.2	Utility Q inductive [kVAr] // read from Amplifier screen
.935	Actual power factor after rounding QL
111.5	P value from Amplifier Screen
41	Q value from LabView Utility Screen
	Configure load composition in RTDS and run it on grid voltage (not internal voltage)
116.2	Enter measured P from the runtime screen into cell A8
48.6	Ditto for measured Q into cell A9
	Disconnect RLC capacitors if any and set the amplifier "Local VAR Ref" = 0
	Run GE amplifier without any PV
	Adjust LimRTDS to get Utility P approximatelly equal to 120kW. Set that value as the Max value on the slider.
	Record Utility P[kW] from Labview into cell A1
	Ditto for Utility Q[kVAr] into cell A2
	Switch back to TestPlan tab (Sheet)

Figure 5-4 Example "Definitions" sheet – part of the TestLog spreadsheet for Sumer05 load composition

Next, the reactive power of the load is adjusted to result in the power factor of 0.95 inductive by providing the desired reactive power reference to the Amplifier. Three things are worth mentioning here:

a) The power factor correction is made to the load if and only if its power factor is lower than 0.95 inductive. If it is higher, no correction is made.

b) The correction is implemented by allowing more of the Amplifier's harmonic filter capacitor current to flow un-cancelled. As was discussed earlier, the measurement system of the amplifier was modified to introduce direct measurement of the current drawn by the capacitance of the AC output filter. Normally, the measured capacitor current is cancelled by the Amplifier closed-loop current control to eliminate its contribution to the load current and make the load current equal to the references supplied by the load model in RTDS. However, when the reactive compensation is desired, a part of the capacitor current matching the desired reactive compensation is not cancelled. The prorating of non-cancelled part of the current is based on the reactive rating of the filter capacitance and its measured current, making the reactive compensation a true function

of physical capacitance, not a calculated value of current that would be based on measured voltage.

c) Related to the last point, if the desired reactive correction is greater than the rating of AC capacitance would allow, a physical capacitance is inserted external to the amplifier to offset the capacitive demand and bring the reactive compensation by the Amplifier back to within the range allowed by its filter capacitance. This allows the test to have a Vernier control of reactive compensation at any operating point.

Next, the predetermined group of solar inverters is brought on-line and monitored within LabView interface to confirm that their aggregate power output matches the planned operating point. This is an important step as some of the inverters within test take several minutes to reach the power output, and their output is contingent on the proper operation of their corresponding DC power supplies. In addition, switching inverters in and out requires energization of their output transformers, which on occasion may result in inrush tripping of the transformers. The test engineer watches the equipment as it goes through its startup sequence and overcomes any equipment problems that may arise. The consolidated feedback and control interface from the LabView program is the key asset during this task.

Once the desired operating point is reached and confirmed by instrumentation, the test engineer initiates the islanding test by operating a “control button” on the LabView screen. This begins data-write to a file, operates the islanding contactor, and continues the recording until the voltage on the island collapses or the timeout is reached. It is worth noting that all islanding tests performed in the project ended on voltage collapse condition.

Another thing worth noting is that the Amplifier plays an indirect role in how tests end. Namely the Amplifier was programmed to disable all protection functions normally available in GE solar inverters, which was necessary to prevent interaction of the Amplifier with the test. It was found, however, that leaving the Amplifier operational after the PV inverters have tripped results in an unstable interaction between the load model in RTDS and the resulting voltage on the Amplifier's harmonic filter. Namely the Amplifier tries to pull the load current from its own filter capacitor, which results in voltage on the capacitor, which then results in RTDS load model responding to that voltage and creating current references. This process repeats unabated and ultimately results in heavily distorted currents in the filter capacitors which damage the capacitor fuses. After damaging a set of fuses in commissioning, this effect was prevented by introducing a special protection feature to the Amplifier control code which trips the Amplifier once the load power is below 5kW. Using the power level as the proxy for detection of PV inverters tripping by the Amplifier is superior to using voltage or current levels or waveforms because after the PV inverters tripping, the voltages and currents created by Amplifier/RTDS interactions have unpredictable waveforms. In contrast, measuring three-phase power provides a reliable signal level regardless of waveform distortion and is inherently accurate because pulling current out of capacitance cannot result in active power.

An additional minor point is worth clarifying for completeness: To prevent interaction of this power-based protection logic with the Amplifier startup, the protection is armed only after the load has reached a level greater than 50kW. Such setup ensures seamless integration with the test. Normally, the amplifier is started connected to the grid and reaches the operating point of ~120kW following the reference currents from RTDS. The protection is armed during load ramp-

up and available to guard the AC filter fuses in the subsequent islanding test. The protection operates when the collective output of PV inverters falls below 5kW, at which point the Amplifier is stopped. Stopping of the Amplifier is also the effective end of an islanding test.

Upon completion of each test the test engineer records the file numbers saved by LabView and any notes in the TestLog spreadsheet. A partial screen-capture of the TestLog spreadsheet is shown in Figure 5-5 and it merits a brief description.

0.1,0.1,0.1,0.0,0.1,0.1,0.1			2) Configure Definitions sheet			3) Save as TestLogSummer01.xlsx {Summer | Winter} {01 | 02 | ...} Season and priority code						
Operator	DG Code	P3ph (B2) [kW]	Pwall (B1) [kW]	Pgen [kW]	Penetration [%]	RLC [kW]	GE Amp RTDS File	QC load [kVAr]	PF load []	LabView File Nums	Normal?	Comment
6/23/2015												
	xoff a	0	31.2	31.2	26%	119.6	n/a	5.9	.950		s	LimRTDS = 0.96, Local Var Ref = 5900, Passive Cap = 0
AXEy	xoff b	0	42.8	42.8	36%	119.6	n/a	5.9	0.95	599-600	y	
AXEy	x45 a	42	31.2	73.2	61%	119.6	n/a	5.9	0.95	597-598	y	
AXEy	x45 c	42	53.4	95.4	80%	119.6	n/a	5.9	0.95	595-596	y	
AXEy	x100 b	76	42.8	118.8	99%	119.6	n/a	5.9	0.95	593-594	y	
AXEy	x100 c	76	53.4	129.4	108%	119.6	n/a	5.9	0.95	591-592	y	
	x100 d	76	62.4	138.4	116%	119.6	n/a	5.9	0.95		s	
	xoff a	0	31.2	31.2	26%	119.6	n/a	20.9	.980		s	LimRTDS = 0.96, Local Var Ref = 20900, Passive Cap = 0
AXEy	xoff b	0	42.8	42.8	36%	119.6	n/a	20.9	0.98	609-610	y	
AXEy	x45 a	42	31.2	73.2	61%	119.6	n/a	20.9	0.98	607-608	y	
AXEy	x45 c	42	53.4	95.4	80%	119.6	n/a	20.9	0.98	605-606	y	
AXEy	x100 b	76	42.8	118.8	99%	119.6	n/a	20.9	0.98	603-604	y	
AXEy	x100 c	76	53.4	129.4	108%	119.6	n/a	20.9	0.98	601-602	y	
	x100 d	76	62.4	138.4	116%	119.6	n/a	20.9	.980		s	
	xoff a	0	31.2	31.2	26%	119.6	n/a	45.2	1.0		s	LimRTDS = 0.96, Local Var Ref = 45200, Passive Cap = 0
AXEy	xoff b	0	42.8	42.8	36%	119.6	n/a	45.2	1.0	621	y	
AXEy	x45 a	42	31.2	73.2	61%	119.6	n/a	45.2	1.0	619-620	y	
AXEy	x45 c	42	53.4	95.4	80%	119.6	n/a	45.2	1.0	617-618	y	
AXEy	x100 b	76	42.8	118.8	99%	119.6	n/a	45.2	1.0	614-616	y	
AXEy	x100 c	76	53.4	129.4	108%	119.6	n/a	45.2	1.0	611-613	y	
	x100 d	76	62.4	138.4	116%	119.6	n/a	45.2	1.0		s	
	xoff a	0	31.2	31.2	26%	119.6	n/a	69.5	.980		s	LimRTDS = 0.96, Local Var Ref = 20400, Passive Cap = 49.1
AXEy	xoff b	0	42.8	42.8	36%	119.6	n/a	69.5	0.98	630	y	
AXEy	x45 a	42	31.2	73.2	61%	119.6	n/a	69.5	0.98	628-629	y	
AXEy	x45 c	42	53.4	95.4	80%	119.6	n/a	69.5	0.98	626-627	y	
AXEy	x100 b	76	42.8	118.8	99%	119.6	n/a	69.5	0.98	624-625	y	
AXEy	x100 c	76	53.4	129.4	108%	119.6	n/a	69.5	0.98	622-623	y	
	x100 d	76	62.4	138.4	116%	119.6	n/a	69.5	.980		s	

Figure 5-5 TestLog spreadsheet for Summer05 load composition

At the top of the figure is the row of values shown in red text that provides a reminder to the test engineer on how to generate the TestLog file from the TestLog file template. This is done once per load-composition and before iterations of reactive compensation and PV penetration.

The main body of the TestLog spreadsheet is organized to follow the test procedure laid out in Figure 5-2: Groups of rows represent the desired load power factors, while rows within groups represent the PV penetration levels. The template has a provision for seven penetration levels, but only five, shown with green background, are actually used. The other two, with white background, are skipped. Measured values of load P and Q recorded earlier in the Definitions sheet are used to calculate the necessary additional reactive compensation for each group – captured in "QC load [kVAr]" column. In the example of Figure 5-5, an additional 5.9kVAr needs to be added to the load to achieve 0.95 inductive power factor. The test engineer will have achieved this by entering 5900VAr of reactive compensation on the Amplifier control screen (not shown), as is documented in the note of a skipped test in the first group.

As individual tests are performed, the test engineer records the file numbers saved by LabView for each islanding test. In addition to this, the test engineer may also enter a note if anything during the test seemed out of ordinary.

Once the group of islanding tests is completed for a given value of load power factor, the test engineer "screens for acceptance" – step 7) in Figure 5-2. The screening involves automated processing of test results to prepare plots of waveforms for the group of completed tests. The engineer inspects the plots for anomalies and enters a judgment-based "Normal?" qualifier into test log. The values of "Normal?" qualifier are limited to the following set: "y" – yes, "n" – no, "?" – needs additional review, "r" – repeat, "s" – skipped, and "t" – timed. The non-obvious values of the qualifier are "r" and "t". The repeat choice means that the test engineer decided to immediately repeat the related experiment. This might arise if a wrong condition was

spotted in the data – perhaps a group of inverters was not in service resulting in wrong PV penetration. In such case a note is entered to document the problem and the test is repeated before the next group of tests is performed. The timed choice is the provision within the TestLog template to perform characterization tests that do not involve opening of the islanding contactor. The same TestLog spreadsheet was used in a broader context during system commissioning, so this choice was left-in for generality.

Entering the choice of a qualifier automatically applies the background color to the relevant row, which provides a visual confirmation of completed tests and draws attention to abnormal ("n" – marked in red) or suspicious ("?" – marked in yellow) experiments. An example of TestLog spreadsheet is provided as a file accompanying this report.

Chapter 6

Summary of Completed Experiments

The experimental work covered four groups of tests:

1) **Commissioning tests**, aimed to ensure that all equipment is installed correctly and functioning according to plan. Commissioning of the Amplifier was a major effort because much of the control code (firmware) had to be re-written and carefully put into service to minimize risk of damage to the Amplifier hardware.
2) **Characterization tests of hardware**, aimed to:
    a. Confirm operating ranges of different equipment groups: PV inverters, Amplifier, and passive loads;
    b. Verify that the islanding behavior of PV inverters and the RTDS-run Amplifier matches the behavior of PV inverters with the passive load. This constitutes the key acceptance test for the Amplifier.
3) **Characterization tests of RTDS load models**, aimed to confirm that the load models are implemented correctly with respect to trip/reconnect and stall logic. The majority of this testing is achievable in RTDS software using measured voltages from potential transformers. However, we also performed islanding testing of intrinsic load models

where PV inverters were islanded with the load model of just one kind to aid in the understanding of importance of load blending to islanding behavior. Motor B was tested extensively as it represents large motors with significant inertia and was deemed to be the key candidate for non-detection.

4) **Production tests** used to capture islanding behavior of PV inverters and loads according to the test plan of Figure 5-2.

To describe the test results it is necessary to first introduce and explain how the test data was processed to quantify variables of interest. Doing that in this report would take away from completeness of the accompanying report [3] covering data analysis and key findings from the laboratory experiments.

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